Current dumping review – 1

Crossover distortion is a problem in designing any class B audio amplifier. Bias current provides the basis for the usual solution, but introduces the threat of thermal instability. Current dumping is an alternative to bias current, aiming to abolish crossover distortion without further difficulty.

by Michael McLoughlin

In his original article in this periodical (December 1975), P. J. Walker explains a new technique for abolishing crossover distortion in audio amplifier output stages. His ideas are backed by the commercial success of the Quad 405 amplifier, and the subsequent 1978 Queen's Award for technological achievement.

Seven years have now passed, but the discussion continues unabated. The early contributions in these pages were from practitioners in the audio field, including many well-known names, while later material has come from universities over the world. This article presents in good order the results so far obtained. The discussion reads rather like an epic, full of sudden reversals of fortune.

As the new method is often referred to as something of a mystery, it will first be related in terms of familiar ideas. Walker's own explanation is in terms of the circuit of Fig. 1. For small output currents the driver amplifier A itself supplies the load Z_L directly, via Z_3. Larger currents turn on a dumper, and as Z_4 is chosen to be small the dumper then supplies the bulk of the output current. Then A never has to supply much power, and so it can operate in class A, with no crossover distortion. Indeed, A is just the usual driver amplifier, and we shall refer to it as such.

It is therefore appropriate to call the output transistors in Fig. 1 the "current dumpers", and the substantial distortion which remains will be their crossover distortion. Walker has shown how to choose circuit values that result in complete cancellation of this distortion. It is this choice which is the heart of the matter.

Feedback explanation

To start detailed discussion of Fig. 1 with an intuitive idea of its working, that offered by P. Baxandall (July 1976) relies on the most familiar ideas.

He starts from a circuit similar to that of Fig. 2, with S_1 closed and Z_4 shorted as drawn. Now imagine Z_3 removed. There will be no feedback, and the V_{out}/V_{in} characteristic will look like that of Fig. 3, except that the central segment will be horizontal. This occurs while V_{in} makes progress across the dead region, while the output of A is traversing the voltage gap between the levels required to drive the transistor bases. Adding Z_3 assists matters: while this gap is being crossed there is still some output to the load, as shown by the reduced but positive slope of the central segment.

Now open S_1 of Fig. 2, to provide 100% voltage feedback to A. The variation in open-loop gain shown will be violently assaulted, and the ratio of the gains in the dumpers-off and dumpers-on regimes will be very close to unity. There is now scarcely any crank between the three segments of Fig. 3. (Also the horizontal scale has changed dramatically.)

Baxandall observes that there is now a way to make all three segments line up perfectly. All that is needed is a little extra feedback in the dumpers-on regime, to reduce the gain slightly to that found at the central segment. Then the outer segments tilt gently on their point of meeting with the central section, to provide a perfect straight line!

To provide the extra feedback it suffices to remove the short on Z_4. When the dumpers are off this resistor has no influence on feedback, but when they are on the hotter end of Z_4 carries more output voltage than the load itself. So there is now extra feedback when the dumpers are on, as required. Naturally, Z_4 must be chosen with care to produce just the correct flexing in Fig. 3.

If desired, Z_2 may be connected between N and B in Fig. 2. It is however clearly quite unnecessary. Indeed its contribution to total feedback at N is retrograde, actually feeding back more of V_{out} when the dumpers go off. But if Z_2 is inserted, its harmful effect can readily be cancelled by an increase in Z_4, to boost the desired feedback as necessary.

When the correct Z_4 is in circuit the transfer characteristic is perfectly linear. As a result the grounded terminal of the signal source V_{in} may now be connected instead to V_{out}, and the signal source made to float. Of course, much less signal will now be required for a given output.

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Following Baxandall closely we have arrived at Walker's circuit in Fig. 1, with S_1 as drawn. And when S_1 is switched the essential invention now appears as the introduction of Z_4, to provide a little extra feedback in the dumpers-on regime to counter the extra gain introduced into the system when the dumpers bypass Z_3.

Algebra

Baxandall's intuitive explanation can easily be extended into algebra, to derive the Walker balance condition on the four bridge components. The discussion will now centre on Fig. 1, taking the floating "zero volts" rail as zero for the discussion of all voltages. It should be helpful initially to think of this line as "earth", and to regard Z_3 and Z_4 as amplifier load resistors connected to this.

We shall study the total load current I flowing to "earth", and deduce the balance condition in three short paragraphs. Before starting define F as that fraction of output voltage across Z_3 fed back to the negative input terminal of A. And recall that for an amplifier of infinite gain the closed-loop gain is inversely proportional to F.

(A) When a dumper is on, its base-emitter junction cannot support voltage variations, so F=1. But when the dumper goes off the junction is an open circuit, and $F=Z_1/(Z_1+Z_2)$. So F has been multiplied by this last fraction. As A has infinite gain, the closed-loop gain to B promptly multiplies by the inverse fraction, namely $1+Z_2/Z_1$.

(B) However, as the dumper goes off the load impedance which controls I rises from $Z_3\|Z_4$ to Z_3. Dividing, we see that load impedance has been multiplied by $(Z_3+Z_4)/Z_4$, which is $1+Z_3/Z_4$.

(C) There is no charge in gain through to I when the dumper goes off if the gain multiplies by the same factor as the load impedance. The relevant factors are at the ends of the two previous paragraphs, and concur if the Walker condition is met:

$$Z_2/Z_1=Z_3/Z_4 \qquad (1)$$

Actually the argument neglects two minor factors. When F was established for the dumpers-off condition in (A), the effect of Z_4 on the potential division was neglected.

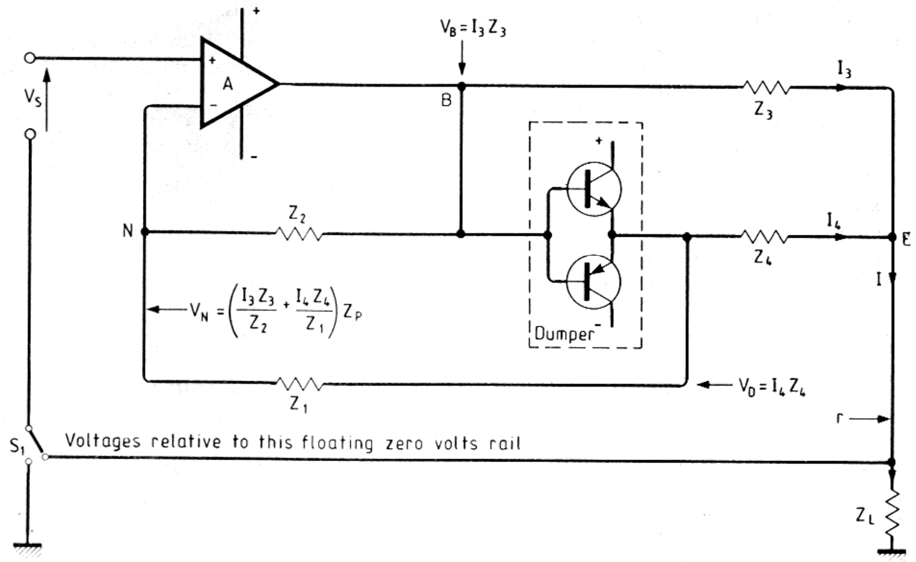


Fig. 1. Walker's basic current dumping circuit. It is a standard class B circuit with elaboration of the feedback network, and floating signal source. (Z_p means Z_1/Z_2)

It should be added to numerator and denominator in the fraction for F. Secondly, when the dumpers go off the output impedance is not exactly Z_3 as stated in (B); there is a second parallel path, and the symbols $\|(Z_2+Z_1+Z_4)$ must be juxtaposed to Z_3. Both these factors are clearly minimal. In fact some straightforward reworking of the argument now shows that they cancel out perfectly, proving (1) exactly. So much cancelling suggests that we are not yet looking at the problem in the simplest possible way.

Lifting the circuit up and down on the floating rail cannot falsify V_s, by definition of that quantity. Nor will it disturb the inputs to A, both of which are carried up and down together. But it will normally falsify the output volts of A, because any amplifier delivers its output relative to its negative rail, and not with respect to a hot point chosen for our convenience in the calculation. In this case, however, we can take refuge in the infinite gain of A. Fig. 4 should make the point clear.

Bridge explanation

It is now clear that with current dumping there need be no gap between intuition and algebra: one passes naturally into the other. It has to be admitted, however, that the argument so far has depended on a simple on/off transistor model, which is not really valid at the edges of the crossover region. We assumed that the base-emitter junction of a dumper either clamped like a short circuit, or passed no current as an open circuit. But the level of intuitive understanding can be extended to include the edges of the crossover region as well, most simply by using an idea of Vanderkooy and Lipshitz (June 1978).

They model the dumpers of Fig. 1 as a voltage source V having zero internal impedance, but varying throughout the cycle just as does the real dumper V_{be}. They then redraw the circuit as a bridge, Fig. 5. The current envisaged as flowing through V in that figure is the dumper emitter current.

Actually only the base current flows in the upper battery arm, but this difference can be ignored as A has zero output impedance. Otherwise the voltages and currents remain undisturbed by the substitution of this "battery". Reduction of current in the upper battery arm is noted by Vanderkooy and Lipshitz as a flaw in their argument. This is because their amplifier has been taken as a perfect current amplifier with infinite output impedance, and so alteration of its output current is unthinkable. Then there is no way of tidying up the current discrepancy, and it follows that in their model the potentiometer rules we are about to use can have no validity.

Suppose now that an arbitrary increase ΔV arises in V of Fig. 5, quite unrelated to the input V_s which remains unaltered for the moment. Well, V_s has not changed, and the voltage between the input terminals of A must remain zero, so V_N remains unchanged. (A can readily secure this by raising the potential at B suitably, while the voltage at D falls sufficiently to make up the remainder of ΔV.)

Now the point E delivers current I, and that current may be calculated on the basis that E is a generator of the e.m.f. that would arise there if the line to I were cut, while the volts at B & D were unchanged. The generator must also be thought of as having output impedance $Z_3\|Z_4$.

Then the output current I will not change if the open-circuit e.m.f. just mentioned does not change in response to ΔV. We know that the change at V_N was zero, so in requiring zero change of this e.m.f. we are simply requiring a bridge balance: $Z_2/Z_1=Z_3/Z_4$.

Meet this condition. Then arbitrary changes in V do not affect output current. If this is true for arbitrary changes of V, then it will be true for that particular track followed by V during the signal cycle. This completes our first rigorous proof of the Walker balance condition (1), where any transistor behaviour is allowed for, even that found at the corners of the crossover region.

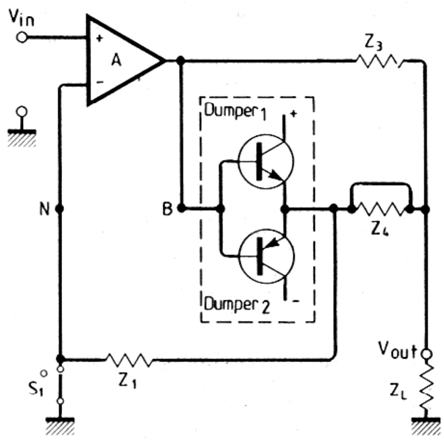
The proof can readily be extended to the real case, where A is finite. When ΔV arises, the amplifier will again control the redistribution of potentials. Indeed for every millivolt that V_N falls, the amplifier will insist on a rise of A (mV) at B. Thus the point of zero voltage change is no longer at V_N, but is $1/(A+1)$ of the way up Z_2. So the open-circuit e.m.f. at E mentioned above will not change if

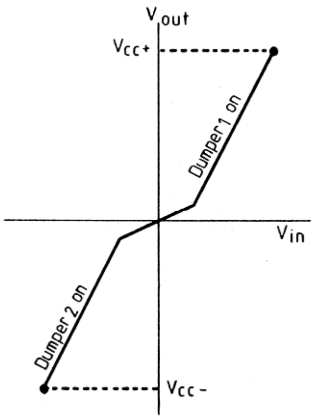
$$\frac{Z_3}{Z_4}=\frac{\frac{A}{A+1}.Z_2}{Z_1+\frac{1}{A+1}.Z_2}. \qquad (2)$$

Thus even when A is finite there is no difficulty in choosing Z_4 to obtain perfect freedom from dumper distortion. Of course (2) can be tidied in various ways. Notice that when A becomes large it tends to (1).

When V_N falls 1 mV, B rises A mV, both measured relative to the floating zero volts rail of Fig. 5. This floating rail causes no embarrassment to the inputs of A, which are both equally affected. But in fact the output of A is produced relative to its negative supply rail, and not relative to any floating rail. This time the difficulty can be deflected by observing that our condition sets ΔI=0, so no voltage difference arises between "zero volts" and ground.

It is still essential to assume zero output impedance in the driver amplifier, to cope with the varying deficiencies in the upper battery arm current as ΔV arises. Of course in a voltage amplifier this output





***Figs 2 & 3.** When Z_3 is present in this class B output circuit the output transistors could be called "current dumpers" just as in Fig. 1. Transfer function is shown bottom at Fig. 3.*

impedance will be very small. In terms of algebra this bridge model is very powerful, and also in terms of intuition. Fig. 5 with an inductor at Z_4 and a capacitor opposite shows that the basic idea is just to balance a traditional LC bridge, according to $L=R_1R_3C$.

Feedforward explanation

It may seem strange that current dumping claims to cancel distortion completely. Certainly in normal correction of error by negative feedback the distortion can never be totally eliminated because a residue must be left to be sensed and so drive the amplifier into opposing the source of distortion. But what if one sensed the distortion in the output current (by comparing it with input voltage) before it was fed into the load, and then injected a further correction current into the load, but forward of the sensing element? The difficulty disappears, because correction does not now reduce sensing and so perfect cancellation of error is then theoretically possible. For example, the crossover distortion of a heavy-duty class B amplifier can be corrected perfectly in principle by a small class A amplifier of high quality.

In practice resistor tolerances do impose serious limitations, though these do not often seem to be analysed. In contrast to feedback, this type of error correction is called feedforward, and has sometimes been aired here (May 1972, October 1974, twice in May 1978). But suppose only four 5% resistors are used in the defining chains. Then the correction may be 20% out. One would do better to increase the

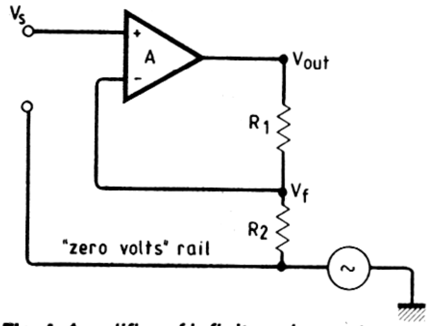


***Fig. 4.** Amplifier of infinite gain must produce V_f equal to V_s even when a voltage source drives the floating "zero volts" rail with respect to which these quantities are measured. Think what would happen if V_f fell short.*

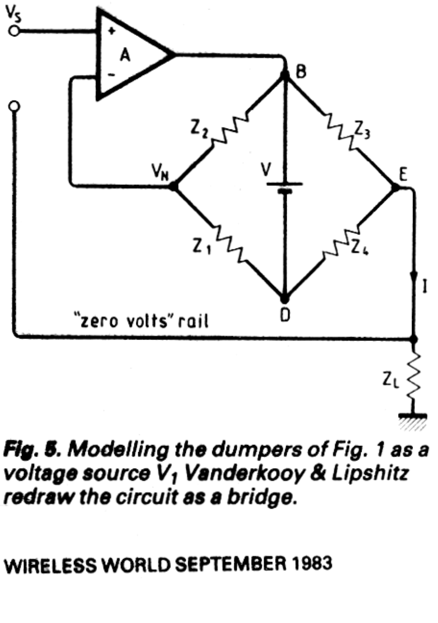


***Fig. 5.** Modelling the dumpers of Fig. 1 as a voltage source V_1 Vanderkooy & Lipshitz redraw the circuit as a bridge.*

gain of the main amplifier by a factor of five, and then use feedback to cut it back again. And this is a great deal easier to do. Nevertheless, the idea of feedforward demonstrates that a claim to perfection of error correction is not objectionable in principle.

Does current dumping use feedforward? Following Baxandall we have presented it entirely in terms of feedback. Imagine Z_4 of Fig. 1 shorted: then the transfer characteristic returns to the style of Fig. 3. The solution was to consider the slope of the central section as basic, and to insert just the right Z_4 to adjust into line the gain of the outer segments. The picture is one of negative feedback being adjusted during the cycle, to make the gain conform to its value at the centre. This is not classical feedback, because the feedback fraction is varied during the cycle, but it is negative feedback, and no further picture is required.

Walker's explanation

In his original article, however, Walker gives a perfectly valid discussion of Fig. 1, which is entirely feedforward in style. He regards Z_4 as the output sensing element, and compares V_s with the sensor voltage I_4Z_4. His argument may be simplified and presented as follows.

A is taken to have infinite gain, so the voltage between its input terminals is zero. Now think of both input terminals as a new "zero volts" point for reference. Viewed from here, $-V_s+I_4Z_4$ appears at the far end of Z_1. As usual when such a signal is fed to the negative input terminal of an amplifier, it reappears at the output terminal but multiplied by $-Z_2/Z_1$. To obtain this output voltage relative to the floating rail of Fig. 1, it is only necessary to add V_s again. (Ignore the expression V_B in Fig. 1.)

So $V_s-I_4Z_4$ is heavily amplified, and if I_4Z_4 is at all sluggish in following V_s a large protest voltage will appear at the output of A, forcing extra current through Z_3 forward of the sensing element Z_4. We have just found the output voltage, so we may choose Z_3 and then write down I_3. Then add I_4 to obtain the total output current, which is just

$$\frac{1}{Z_3}\left[\frac{Z_2}{Z_1}(V_s-I_4Z_4)+V_s\right]+I_4.$$

It is now clear that if Z_3 is chosen according to (1) then I_4 actually cancels out in this expression! Whatever particular I_4 the dumpers choose to allow at any particular time, the output current will remain untouched, provided just the right Z_3 has been fitted.

The language used here is entirely feedforward, though the situation is not classical, for two reasons. Firstly, the protest volts generated by A do actually power the sensing element Z_4 as well as the sensor bypass Z_3. Also Z_3 is not a pure bypass element, but reports back to the amplifier via Z_2, as can be seen clearly in the dumpers-off condition.

Mr Walker's accompanying discussion seems to take as basic the gain when the dumpers are on, feeding current through $Z_3||Z_4$. Of course there will be a short departure from these arrangements during crossover. And during this brief period of error a suitable correction will be fed through Z_3. The whole picture is perfectly valid, and indeed nothing more than this feedforward is required to explain current dumping.

Much binding

Suppose a tuned circuit is energized at its resonant frequency. Then the circulating current is large, compared with its value at adjacent frequencies. Bloggs explains that this is because C is cancelling the high impedance offered by L. Smith objects that this could not be more false. It is L that is cancelling the high impedance offered by C! And so they rattle on.

Obviously high farce has effected an entry. This illustration establishes the principle that a complex situation may sometimes be viewed quite validly in alternative ways. In this case the fullest understanding seems to be obtained when one has seen both explanations, seen that they are both valid, and grasped that they are complementary views of the same situation.

There seems to have been a similar division of opinion about the operation of Walker's amplifier: does it use feedback or feedforward? In good part the discussion seems to stem from a resolve to class a new and hybrid idea as one or the other of the two existing categories. But a major factor might be a failure to realize that a complex idea can sometimes be explained in several different ways. Our own view is that current dumping may be adequately explained by feedback, or by feedforward, or as a bridge, or as a measuring instrument (see below).

Everyone agrees that use of (1) aligns the three segments of Fig. 3. But it is fruitless to argue whether this is because the correct Z_4 has been chosen to make the outer segment slope equal to that found at the centre (feedback), or because the correct Z_3 has been chosen to ensure that the central section slope concurs with the outer parts (feedforward). We followed Baxandall initially as a matter of taste (indeed so does Walker in November 1976): the feedback ideas involved are more familiar.

In their most recent article (cited later) Vanderkooy and Lipshitz again insist that feedforward alone is the only correct explanation. Their argument consists of a logical structure presenting a "conceptual development of current dumping from feedforward." But one has to ask "whose concepts?" An equally clear set of concepts is the basis for Baxandall's feedback explanation. (It is a mistake to list Baxandall's letter here in support of feedforward.) In short, an explanation in terms of feedforward, however clear, does nothing to exclude other explanations.

An objection

In Fig. 1 the value of Z_4 is carefully chosen to yield the correct additional feedback when the dumpers are on. But how can a single value of Z_4 cancel perfectly the

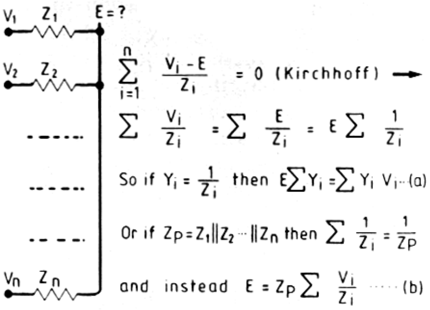


Fig. 6. Millman's theorem allows ready calculation of the voltage E at which a junction will settle. Strictly speaking it is result (a), stated in terms of admittances, and it is useful to abolish denominators in difficult algebra. Form (b) is more useful in easier cases.

peculiar vagaries of dumper V_{be}? And how can anyone assert such a thing without examination of the vagaries concerned?

The objection could easily be met by observing that the result is already secured by different thinking. But it can also be met directly and on the intuitive level by presenting the circuit as a measuring instrument. The dumper behaviour from instant to instant is measured by Z_4, which controls the feedback accordingly to hold the gain constant. Naturally any talk of gain variation within a cycle refers to incremental gain. This intuition is built into a rigorous proof below. We shall not impose the detail on the printer, and all except enthusiasts are urged to bail out at once, as far as the next heading.

Replace the dumpers of Fig. 1 by a resistor R, to stand for the small-signal emitter input resistance of the operating dumper; this variable R connects from Z_2 to Z_4. Now measure all voltages relative to the floating zero rail. Then for unit increment of V_B there will be an increment of V_N given by

$$\frac{Z_4+\frac{Z_1}{Z_1+Z_2}[R//(Z_1+Z_2)]}{Z_4+R//(Z_1+Z_2)}.$$

Add 1/A to this to yield ΔV_s. Now the ΔI resulting from the unit change in V_B is just the reciprocal of the impedance from B to E: write down this simpler expression. Then solve $\Delta V_s=K\Delta I$ in such a way that K does not depend on the varying R. This constant proportionality will provide an undistorted output. Provided it is noticed early that R only occurs as $R\|(Z_1+Z_2)$ and this quantity is labelled x, a page of work will produce a rigorous proof of (2). This time, Z_4 has been regarded as a measuring instrument, noting how much current R passes in response to changes of voltage at B, and then controlling gain accordingly.

There is the usual fallacy in that argument, which it is easier to correct after deriving the result. If the output volts of A rise one unit relative to the floating conductor, then relative to true ground they rise an additional $Z_L\Delta I$. This must be taken into account when calculating ΔV_s, which must therefore be augmented by a further $Z_L\Delta I/A$. But this addition does not contain R and is already proportional to ΔI, so provided K has the value found as above a relationship of proportionality will still prevail between ΔV_s and ΔI.

This analysis is really an extension of Baxandall's feedback approach, showing that it can be extended to include any transistor behaviour, even when A is finite.

Algebraic explanations

In an attempt to dispel mystery the above-mentioned arguments have remained close to intuition, even at the cost of complexity. But we shall now study straight algebra, and discover much simpler arguments.

The obvious method of studying Fig. 1 is to regard Z_2 and Z_1 as a potential divider, whose lower end is at I_4Z_4 volts and whose upper end is maintained a further $I_3Z_3-I_4Z_4$ volts higher. Ignoring the expression in Fig. 1 an expression for V_N is therefore

$$I_4Z_4+\frac{Z_1}{Z_1+Z_2}(I_3Z_3-I_4Z_4).$$

Take A large: then this can be taken as an expression for V_s and tidied:

$$V_s=\frac{Z_1Z_3I_3+Z_2Z_4I_4}{Z_1+Z_2}$$

Suppose now $Z_1Z_3=Z_2Z_4$ as in (1). Then the coefficients of I_3 and I_4 are equal in this expression for V_s. So the output current (I_3+I_4) has been locked into a proportionality relation with V_s, and the output is undistorted.

An even briefer analysis seems to underlie the remarks of J. Halliday (April 1976). He appears to rely on the circuit theorem of Fig. 6, which gives in two convenient forms the potential adopted at the meet of several impedances. We shall rely heavily on this theorem henceforward.

When Fig. 6 (form b) has been mastered, it will be easy to verify the expression for V_N marked in Fig. 1, where only two arms Z_1 and Z_2 are connected to marked voltages. Now $V_s=V_N$ because the gain of A is large. Simply by looking at that expression for $V_s=V_N$ it is clear that if $Z_4/Z_1=Z_3/Z_2$ then V_s and (I_3+I_4) are trapped in a linear relation.

Given the expressions of Fig. 1, the last sentence provides a fifth proof that cancellation of distortion is possible, and gives the condition for it.

Output current

For practical reasons Z_4 is much smaller than Z_3, and provided the balance condition holds then

$$Z_3\gg Z_4\Rightarrow Z_2\gg Z_1\Rightarrow Z_P\approx Z_1$$

(Strictly speaking the first four symbols should have modulus signs.) So the $V_s=V_N$ of Fig. 1 now simplifies to

$$V_s=V_N=(I_3+I_4)\frac{Z_4}{Z_1}.Z_P$$

and if $I=I_3+I_4$ we have

$$V_s\approx IZ_4 \qquad (3)$$

In other words the output current can be calculated simply by supposing that V_s is applied to Z_4, and it can be modelled by the output current I in the emitter follower circuit of Fig. 7 (with S_1 as drawn.)

The operator H

Before entering on our conclusions we have a duty to look at the difficult article of H. S. Malvar (March 1981). Its early algebra can be much simplified, as shown by K. G. Barr (June 1981). The article relies heavily on a multiplier B, which it will be safer here to call H, and it is used to relate two voltages of our Fig. 1 according to $V_D=HV_B$. This H is the most general possible multiplier, and it changes with V_B as necessary, to maintain the above equation true to what happens in an amplifier. Certainly if one makes a printout of these two voltages at small increments of either, then H could be listed in a third column. Indeed for a given amplifier H could be presented as a list opposite small increments of input signal to the amplifier. But of course such a system leaves the list for H violently dependent on any variations in driver gain that are being considered.

Well, briefly, there is no need to consider what happens when H is off-course by ΔH. The course is defined as above by what H does, and it cannot be off-course. ΔH is meaningless and should be set at zero throughout (equation 8 misleading). If this is not liked, then an alternative description of H must be given. Also it is clear from the above equation that one may not reason on the basis that H=0 when the dumpers are off (equation 12 wrong). And when A is allowed to tend to infinity, then his (6) requires either that R_3 does likewise, or R_4 tends to zero (equation 9 wrong). Finally, once it is admitted that a change in driver gain will cause shifts in H, the Maclaurin expansion used is not only incorrectly computed (equation 10 wrong) but quite invalid in method (H has been treated as a constant in the differentiation.)

Quad 405

Walker explains that he takes (1) as the basic design equation for the Quad 405 design, with $Z_1=R_1$ and $Z_3=R_3$, so that both are straight resistors. But Z_4 is an inductor L and Z_2 is a capacitor C. Ingeniously enough, substituting the necessary $j\omega L$ and $1/j\omega C$ in (1) yields nevertheless the frequency-independent balance condition found in the bridge model:

$$L=R_1R_3C \qquad (4)$$

This ensures that the coefficients of I_3 and I_4 found at V_N in Fig. 1 are equal and will stay equal to each other at all frequencies.

But it does nothing to ensure that these coefficients remain constant as frequency varies, and disaster has in fact struck at this point. Indeed, simply by looking at (3) one can see that if Z_4 is an inductor then output current is inversely proportional to frequency. In circuit terms, what happens to the frequency response in Fig. 7 if Z_4 is an inductor?

This conclusion can be confirmed by substituting R_1, $1/j\omega C$, R_3 and $j\omega R_1R_3C$

for the four bridge values in V_N of Fig. 1 and simplifying, to obtain

$$V_N=\left[\frac{j\omega R_1R_3C}{1+j\omega CR_1}\right]I.$$

The bracketed factor is almost constant when ω is large, but its modulus does fall with frequency. Indeed, with $R_1=500\Omega$ and $C=120pF$ as in the Quad 405, the denominator is essentially unity below 1MHz. Hence V_N varies as f in the audio range, and output varies as 1/f there.

The use of L and C in the bridge has resulted in a ferocious dependence of gain on frequency. The solution applied is the use of massive negative feedback, applied in the usual way by switching S_1 in Fig. 1. This can be modelled by switching similarly in Fig. 7. In this figure Z_4 now causes no attenuation of output across Z_L at low frequencies, but at 20kHz it may reduce output noticeably. Suppose we decide that at 20kHz we will tolerate a 0.1% reduction in output volts. Then if $Z_L=8\Omega$, $Z_4=0.36\Omega$ inductive, so $L=2.85\mu H$. Actually $3\mu H$ is fitted.

Many pairs of L and C would satisfy (4), and there has been no explanation of the choice made. It seems that feedback is unable to overcome the effect on gain if L is any larger, even when the amplifier gain is infinite. It follows that above 20kHz the performance of this amplifier must begin to deteriorate, and this explains the exhortation not to make tests with square waves.

Somersaults

The operation of the circuit in Fig. 1 may now be summarized in a sentence. Firstly bridge values are balanced to ensure that $V_N \propto I$, and then the driver amplifier is used to ensure that $V_N=V_s$, thus locking into proportionality V_s and I.

This full discussion of current dumping equips us to examine the controverted points, and we shall now witness three successive somersaults before the end of this article.

Firstly Halliday, supported by Olsson (July 1976), rides in from the flank. He agrees with all that has been said, but points out that it is entirely superfluous. We have just seen that the method depends on deriving a feedback V_N proportional to (I_3+I_4). Then why not derive it from a small resistor in series with the load at r in Fig. 1?

Indeed, supposing that (1) holds and examining V_N of Fig. 1, the value of r required to give identical feedback voltage is readily seen to be $Z_PZ_4/Z_1 \approx Z_4$. (The accurate figure is $Z_3 \| Z_4$.) And J. G. Bennett (April 1976) drives the nail home. Such an r will provide feedback strictly proportional to I, but Walker's bridge owing to tolerances cannot be expected to balance perfectly the two coefficients in V_N in Fig. 1. The bridge will not produce a feedback strictly proportional to I, and current dumping is actually worse than the simpler conventional approach proposed.

Walker in his reply does not oppose these arguments. He points instead to the real case where A is finite, and quotes result (5) below, in a slightly different algebraical form. The result may readily be derived, by noting that if A is finite then a voltage V_B/A exists between the input terminals of A in Fig. 1. This yields a second expression for V_N, given on the left below and equated to that of Fig. 1:

$$V_s-\frac{I_3Z_3}{A}=\left(\frac{I_3Z_3}{Z_2}+\frac{I_4Z_4}{Z_1}\right)Z_P$$

$$\Rightarrow V_s=Z_P\left[I_3\left(\frac{Z_3}{Z_2}+\frac{Z_3}{AZ_P}\right)+I_4\cdot\frac{Z_4}{Z_1}\right]$$

So V_s is again locked linearly to (I_3+I_4) if

$$\frac{Z_4}{Z_4}=\frac{Z_3}{Z_2}+\frac{Z_3}{AZ_P} \qquad (5)$$

The usual difficulty arises from the floating zero-volts rail of Fig 1. The real output voltage of the amplifier is not just V_B: in fact $(I_3+I_4)Z_L$ needs to be added. Divide by A and use the result to alter the figure used above for volts between the amplifier input terminals. But the extra term has I_3 and I_4 already balanced, leaving unaltered the above balancing requirement (5).

Thus the current dumping circuit can still provide freedom from crossover distortion with finite A. Further, fixing an eye on (5) and examining V_N of Fig. 1, it is now clear that the coefficients of I_3 and I_4 in that expression are no longer equal. Hence V_N cannot now be derived from a resistor in series with the load. Current dumping is sound after all, because Halliday's objection only applies when A is infinite.

But Walker does not go on to revise his explanation of the Quad 405 to show how he has used (5) instead of (1). Indeed, it would appear that he did use the last mentioned. For a start, his explanation is in terms of (1), and also of (4) which is a form of it. Further, the driver in the Quad 405 is a current output device whose working load adopts three values over the cycle. According to (5) there is still a solution: make the gain very large, and then the last term can be dismissed, together with its several gyrations. Then variations in A during the cycle will not upset the bridge balance. Now whether one thinks of A as infinite or merely as large, neglect of the third term of (5) means that the coefficients of V_N of Fig. 1 are set equal. And so identical feedback can be derived from the small resistor mentioned earlier. Halliday's criticism is sound: the Quad 405 would work better without its current dumping. These matters will recur in Part 2.

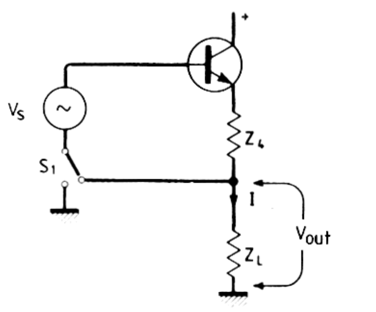


Fig. 7. Dumper output model.

In principle, however, current dumping is now once more of value, provided that A is not taken as large, but is allowed instead to influence (5). The dumpers may do as they please as the cycle progresses, provided only that A is not given too much work. So any crossover distortion caused by the dumpers, or indeed any other harmonics, noise, hum or delays that they introduce into the circuit will all cancel perfectly.

Tolerances

All that is theory, however, and the position is reversed for the third time when practical considerations are taken into account. Components do not have their nominal values, but are produced to tolerances. It follows that if A is large, the designer cannot give any serious weight to the last term in (5), whose contribution will be overrun by tolerance errors in the other terms. He might as well specify $Z_4/Z_1=Z_3/Z_2$, and once this is done Halliday's observation on V_N recovers all its power. Such an amplifier would do better to abandon current dumping.

What sort of amplifier could use current dumping with advantage? Certainly not one where A is so high that the third term of (5) disappears under the tolerance of its predecessor. If this has happened then a designer attempting to allow for the third term will actually do harm to a proportion of his production run. The critical value of A is the figure which reduces the third term in (5) to 10% of the value of the previous term, because the third term is then getting inside the 10% uncertainty of its predecessor. (We are assuming 5% components, as in the Quad 405.)

Indeed the noose can now tighten, if variation of the first term of (5) is taken into account. Now the third term must not fall below 20% of its predecessor. So the critical value of A satisfies

$$\frac{Z_3}{AZ_P}=\frac{1}{5}\cdot\frac{Z_3}{Z_2}\Rightarrow A\approx\frac{5Z_2}{Z_1}\approx\frac{5Z_3}{Z_4}$$

(where really the moduli are under consideration).

We are kinder to current dumping if this upper limit on A is set high. But Z_4 cannot really be made smaller than 0.1Ω, or the resistance of the soldered joints will get into the act. And Z_3 might be 47Ω as in the Quad 405. In which case the upper limit on A is around 2,500 or so. If A exceeds this no designer can allow for it because of tolerances. In particular, the circuit is no use if the driver is an op-amp.

To recapitulate, if A is thought of as large and the last term of (5) neglected, the current dumping circuit is actually worse than normal negative feedback. Indeed, even if A is linear, and known, and used in (5), tolerances defeat the designer's efforts unless A is under 2,500 or so. There might just be a window of gain up to this figure where current dumping could be useful. This point is pursued in part 2 of this article. Meanwhile, it appears that reactive components should be kept out of the bridge.

To be continued

Current dumping review – 2

Current dumping is a circuit technique which claims to abolish all crossover and other distortion caused by a class B output stage. This analysis shows that in precisely this respect the performance of current dumping is notably inferior to that of a traditional amplifier of similar design.

Discussion so far can be summarized by reference to Fig. 8, where V represents the distorting dumper V_{be} and its quasi-rectangular behaviour. Signal input has been ignored as it is the influence of V on E which is to be studied.

The aim is to ensure that variation of V does not affect E. If A is taken as finite this cannot be done by balancing the bridge in the usual fashion. For no change at E then implies no change at C or at B, implying change at E contrary to hypothesis. What is required is for the bridge to be a little off balance, so that when E remains constant a small amount of V is fed back to the amplifier: enough to shift B appropriately. Clearly then the small bridge unbalance required is inversely proportional to the gain A. Algebra will handle the details, and dumper distortion will totally cancel, however V behaves.

As mentioned, taking A as infinite leads to destruction of the system. The bridge would require to be balanced as normal, because A now requires no input voltage. Whence if E is not varying with V the negative input of A might as well be connected to E instead of to C. Then Z_1 and Z_2 can be removed, and Z_4 replaced by a wire.

Previous discussion was based on a floating signal source, which is not attractive. Further, the floating "zero volts" rail required frequent corrections to the algebra. Divan and Ghate (WW April 1977) remove these irritations, and bring the theory to a new level with the circuit of Fig. 9. They include Z_{in} together with the gain-setting element Z_f hinted at by Walker, and take A as finite. Their balance condition (6) is derived in two lines in Fig. 9, and contains all earlier results.

Invalidity

Murmurs have been heard that much of this debate is invalid. Suppose that the output current through Z_L in Fig. 9 is sinusoidal. Then the current marked i through Z_4 supplies most of it, but it is switched off during crossover. Meanwhile I−i flowing through Z_3 supplies what is wanting. Then both of these currents depart dramatically from the sinusoidal form.

Now the interest of this analysis lies largely in the study of the very successful Quad 405 amplifier design that uses the technique. But in that amplifier Z_2 is a capacitor and Z_4 an inductor. When currents and voltages depart from the sinusoidal it is impossible to attach impedance values to these components, and the symbols used above for such quantities have no meaning. Take the case of Fig. 10, where a 'square' voltage wave is

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applied to a capacitor and series resistor. The ratio V/I wanders through most values from zero to infinity throughout the cycle, and there is no constancy about it at all. In these circumstances one may certainly not note the current through C, and divide by $j\omega C$ to obtain the voltage across this component. Fig. 10 certainly presents an extreme case, but if Z_2 is a capacitor it is just the case of Fig. 9. A quasi-rectangular voltage is applied to this component, and the current is to be derived by multiplying by $j\omega C$!

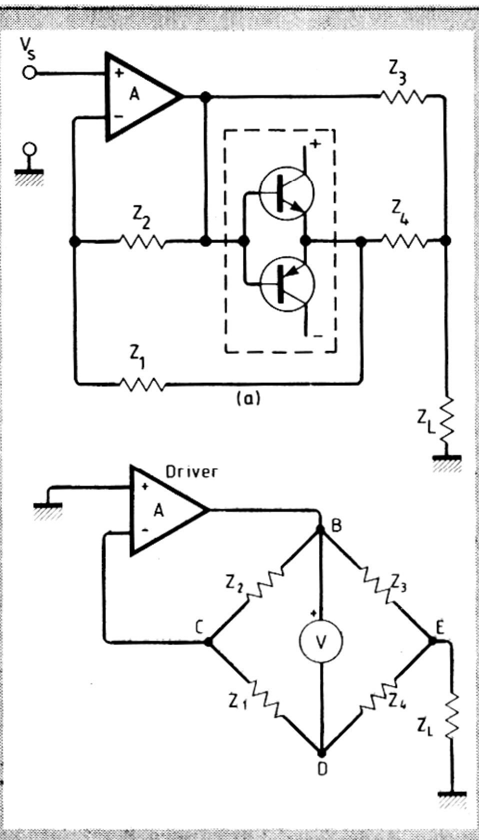
If V in Fig. 10 is a sinusoid then the current I has that form also. If we agree to make comparisons with a certain time delay between these two variables, then a constant of proportionality which does not vary with time will again emerge. And the complex number analysis has been developed to mechanize the accounting. And it would be valid in this circuit to resolve V into sinusoids, use complex numbers on each separately to deduce the consequent I, and add the results. Of course the results would be at different frequencies. But this does depend on the circuit being composed of only linear components, where the output due to a sum of inputs is sure to be the sum of what each would produce separately.

This might be tried in Fig. 9, by

Current dumping

Basic current dumping circuit Fig. 8 (a) may be redrawn as a bridge (b), with the distorting dumper V_{be} modelled as a voltage generator of similar behaviour. Signal can be neglected: it is this voltage generator that can produce no output at E.

Hypothesis: E does not vary when V does. Then it is useless to balance the bridge as normal for no change at E then implies none at C, or at B, resulting in change at E contrary to hypothesis. Slight imbalance at C is required instead. Then if V increases E remains unaltered, but there is a slight fall at C: enough to lift B sufficiently to ensure E is unaffected. The imbalance required is both slight and critical, and the arrangement is very sensitive to tolerance errors.



resolving the currents i and I–i into sinusoids, and discussing each component separately. But Fig. 9 does not show a network composed of linear elements: base-emitter junctions are non-linear in the extreme. This route is barred.

One example of the many possible consequences of reckless resolution into sinusoids is provided by the ordinary a.m. detector. Suppose that such a circuit is supplied with a carrier modulated by a tone. The output is of course the tone, plus a d.c. level. But now resolve the input into sinusoids: the carrier plus two sidebands. Taken separately each of these would produce only a d.c. levels and when added they yield only a d.c. level: the tone has vanished. Conclusion: no detector detects!

Validity

Such criticisms do appear to apply to most of the previous discussion, including of course our own treatment in Fig. 9. However the bridge model of Fig. 8 escapes untouched. Here the troublesome non-linear dumpers have been replaced by a voltage generator, and in determining whether a circuit is composed of linear elements the generators do not have to pass any tests. (Detailed information about the behaviour with time of this generator will be required later.)

Could this trick for turning a non-linear into a linear circuit be applied elsewhere, perhaps in the a.m. detector mentioned above? It can, provided that sufficient information is available about the non-linear voltage V. In the case of the detector the diode must be replaced by V, and when V has to be specified it will be given audio elements suitable for producing the correct output, now that the r.f. cannot yield it. The procedure is valid enough, but in this case scarcely attractive.

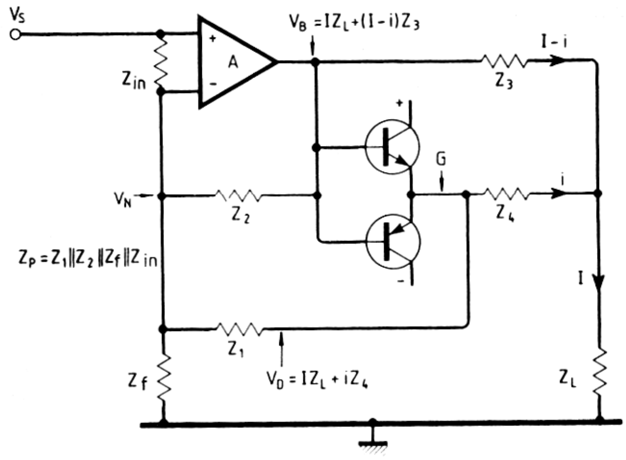
Advance to Fig. 9 again. Replace the dumpers by transistors of constant current gain but zero V_{be}, in series with a voltage generator to be inserted at G. These odd transistors are linear elements: their emitter current in response to a sum of base currents is just the addition of what each would produce separately. And the V_{be} generator may produce such voltage as it sees fit, while the signal at A varies, without violating the linear character now

Table 1. Discontinuity in sinusoidal output E at crossover. Theory provides these figures when tolerances are taken into account. Case 1 offers two transitions per crossover, and the figure in the text has been doubled, as e=0.2 now. Using closer tolerance components would benefit the first two cases equally. Adding bias components would benefit all three cases equally.

Organisation	V pk-pk	Notes
1. As supplied	7.0mV	∝E and ∝f
2. Resistive bridge	0.6mV	at all E and f
3. Traditional amplifier	0.15mV	at all E and f

Transitions at crossover: Quad 405
e=0.2 f=13.2kHz E=1V r.m.s.

Fig. 9. In Divan and Ghate model for current dumping V_B/A must exist between the input terminals of A. So V_N may be derived from V_S. The result is equated below to V_N, as derived by Millman's theorem (proved in Fig. 6):



$$V_s-\frac{IZ_L+(I-i)Z_3}{A}=Z_p\left[\frac{IZ_L+(I-i)Z_3}{Z_2}+\frac{IZ_L+iZ_4}{Z_1}+\frac{V_s}{Z_{in}}\right]$$

This is a linear bond between V_s and I if the terms in i balance out:

$$\frac{Z_4}{Z_1}=\frac{Z_3}{Z_2}+\frac{Z_3}{AZ_p} \qquad (6)$$

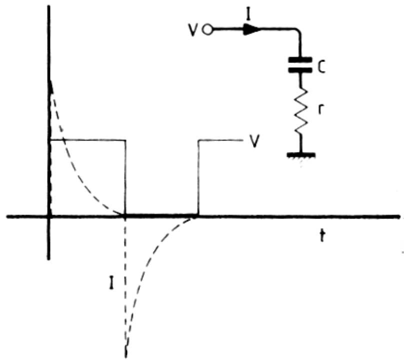


Fig. 10. Current when a rectangular wave voltage is applied to a capacitor and series resistor.

possessed by the network. Naturally we shall oblige G to follow the real V_{be}. The network is now linear, but has two input signals.

When deprived of their V_{be} the two dumpers together make a single linear element. Admittedly a slight violation of linearity will occur on passage from one dumper to the other, because their current gains will not be equal. Apart from this detail, the model now offers a rigorous treatment of the bulky non-sinusoidal currents and voltages in the reactive bridge components. And on a second reading it will be possible to see that this assymetry must degrade a little further the result in the first line of Table 1, thus strengthening our conclusion there.

The two inputs at V_s and G in Fig. 9 may now be considered as sums of sinusoids, and the influence of these on output may be anlysed one frequency at a time. Or V_s and G could be considered separately. And handling one frequency at a time the usual complex number analysis may be employed, with the final output counted as the sum of the separate outputs produced by all these components. Using these tricks a valid proof of (6) can now be given, after the style of what follows.

Quad 405 circuit

The full circuit may be inspected in the operating manual, or in Walker's article Fig. 11 offers his simplified version, with Z_1 to Z_4 clearly marked, and values are attached.

Recall that the generator V in Fig. 8(a) really represents the two complementary dumpers. Their emitters are connected to D and bases to B. So Walker identifies the circuit of Fig. 11 with that of Fig. 8(a). But there is a difficulty. Not only has an extra transistor Tr_2 appeared, but Z_1 and Z_2 are connected to opposite ends of it. Now dumper V_{be} variation will inject current via Z_1 into Tr_2 emitter, and if the driver gain is large this current might just as well be considered as injected into the collector circuit directly. To effect this transfer is just the role of a transistor. Thus if the input signal in Fig. 11 is set at zero, then from an a.c. viewpoint Z_1 can be considered as connected directly to the collector, to identify with the layout of Fig. 8.

But if minimum figures are taken for the gains of the transistors in the driver, its input impedance is about 50kΩ, and during crossover its voltage gain is only about 77. Thus at 1kHz the capacitor C presents an impedance to Tr_2 collector of $Z_C/77$ or 17kΩ. The collector will feed such a load without difficulty. The current is provided by Z_1 = 500Ω, and is injected into the emitter with little difficulty. But that resistor could not be expected to feed 17kΩ without change: Z_1 may not really be considered to be connected to the collector, and Fig. 8 is not an accurate model for the real circuit of Fig. 11.

Vanderkooy and Lipshitz handle the difficulty in just the opposite way, by considering Z_2 to be disconnected from the collector and joined instead to the emitter. Transistor Tr_2 becomes part of the driver amplifier, and the circuit again identifies with that of Fig. 8(a). From the figures

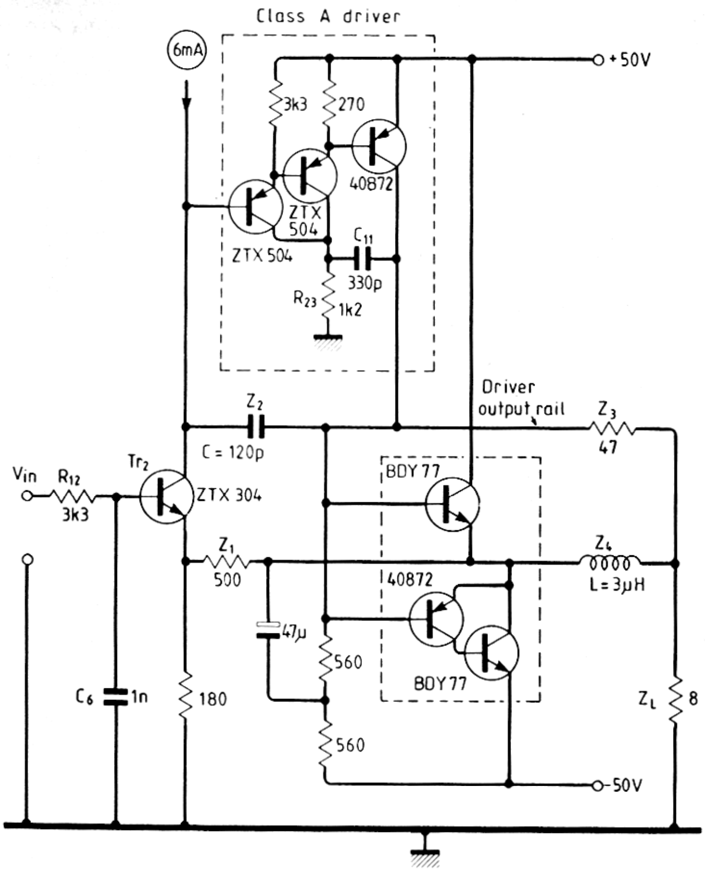
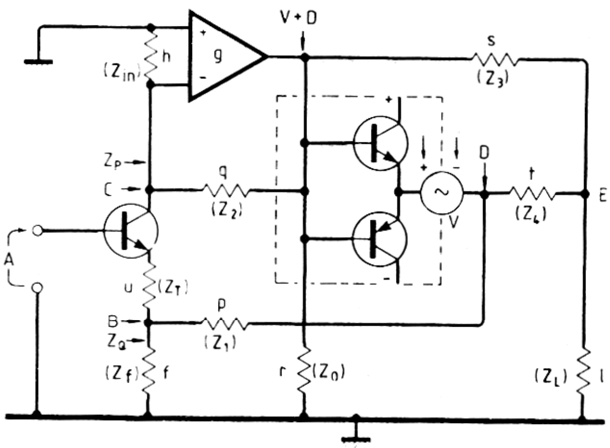


Fig. 11. Walker's simplified circuit of the Quad 405 amplifier, omitting current limiting and h.f. trim components. I have further omitted the LM301A op-amp that provides V_{in}. (It operates in class A, is not part of the current dumping circuitry, and receives only a d.c. feedback – not shown – from Z_L to centre the working point of the dumpers) Minimum h_{FE} for a BDY77 is 40; for the other transistors shown it is 50.

Fig. 12. In this current dumping model A, B, C, D, V denote voltages, small letters admittances.



DEFINITIONS

k: dumper $i_b = k i_e$

$b = q + r + s$

$m = l + s + t$

$n = f + p + u : \frac{u}{n} = \lambda \approx 1$

$g' = g - q$

$Z_P = \frac{1}{h+q};\ Z_Q = \frac{1}{n}$

CONSTRAINTS

$s(V+D-E)+q(V+D-C)+r(V+D)+k[t(D-E)+p(D-B)]=-gC$

(1) $-(s+kt)E=-bV-[b+k(t+p)]D+kpB-g'C : n(s+t)(h+q)$

(2) $(s+t)D=mE-sV;\ nB=uA+pD : (s+t)$

(3) $n(s+t)B=u(s+t)A+pmE-psV;\ (h+q)C=uB-uA+qV+qD : n(s+t)$

(4) $n(h+q)(s+t)C=-u(s+t)(f+p)A+(nqt-psu)V+m(pu+qn)E$

ARGUMENT

Write $wE=xA+yV$ *where* (7)

$w=(h+q)[mn(-s-kt+b+k(t+p))-kppm+nl(s+kt)]+g'm(pu+qn)$

$\quad =(h+q)[mn(q+r)+kpm(f+u)+nl(s+kt)]+g'm(pu+qn)$

$x=u(s+t)[kp(h+q)+g'(f+p)]$

$y=-bn(s+t)(h+q)+[b+k(t+p)]n(h+q)s-kp(h+q)ps+g'(psu-nqt)$

RESULT

$y=0 \Rightarrow g'(psu-nqt)=(h+q)[bnt-kns(t+p)+kpps] : \div g'stn$

$$\lambda \cdot \frac{Z_4}{Z_1} = \frac{Z_3}{Z_2} + \frac{1}{g'Z_p}\left[1+Z_3\left(\frac{1}{Z_2}+\frac{1}{Z_0}\right)-k\left\{1+\frac{Z_4}{Z_1}\left(1-\frac{Z_Q}{Z_1}\right)\right\}\right] \quad (8)$$

Approximate admittances at 1kHz (moduli in mhos)

$p=10^{-3},\ q=10^{-6},\ r=10^{-3},\ s=10^{-2},\ t=50,\ l=0.1,\ f=10^{-2}, u=3\times10^{-2},$
$h=2\times10^{-5},\ g=2.\ 0<k<1/40.$

just given for the driver of Fig. 11 it is clear that above 1kHz it works as an operational amplifier, ensuring that most of the current supplied by Tr_2 is drawn away through C, while leaving only a small amount to work the driver itself. Now as the current gain of Tr_2 from emitter to collector is unity, C could indeed syphon off this current with similar effect at the emitter instead.

But this alteration does obscure an important factor. In Fig. 11 the element Z_1 is marked as 500Ω, but in fact any current due to dumper V variation flowing into Tr_2 emitter is also affected by the emitter input impedance found there. Owing to the presence of R_{12} this may be as high as 3.3k/50 + 25/6 = 70Ω, causing a 14% increase in the effective value of Z_1. If now Z_2 is connected instead to the emitter and there syphons off its current from that flowing into the driver, then scarcely any of the current supplied through Z_1 remains to flow into the emitter. Not much impeding voltage arises, and the 14% adjustment required in the value of Z_1 disappears. If a bridge is to be balanced then a 14% adjustment in the value of one arm is serious, and Z_2 may not be reconnected as proposed in any accurate model of Fig. 11.

It seems possible that Z_1 and Z_2 were initially connected to the same point of Tr_2, but were later separated as part of the h.f. trimming programme evident in the full circuit.

Quad 405 model

Fig. 12 offers a model for Fig. 11. The driver has been reduced to linearity by its specification in terms of mutual conductance. The dumpers are so reduced by thinking of them as transistors of equal current gain but zero V_{be}, in series with a generator to simulate the latter. The driver is equipped with input impedance Z_{in} and output impedance Z_o. Gain-setting element Z_f appears. Delivery of feedback to both ends of Tr_2 is properly represented. Finally Z_T is in series with Tr_2 emitter to stand for the input impedance found there.

The circuit may now be analysed in terms of the two input voltages A and V. Because the components are all linear these may be treated separately, and as sums of sines. Thus complex number analysis is valid. But the twin menaces of this sort of analysis are suffices and denominators. It has been possible to avoid both by giving each impedance a second unbracketed symbol to represent its admittance.

The definitions section of Fig. 12 starts by defining k to account for dumper current gain, and there follow names for concatenations of symbols that will arise. About half the remainder may be omitted at first reading, and the new balance condition (8) can be attained quite quickly.

Constraints

Solving the circuit of Fig. 12 consists in obtaining the relationship between the three voltages A, V and E. To build relationships it has been necessary to introduce voltages B, C and D, so these are to be eliminated.

Observing that the current flowing away

from the driver is equal to what it provides, then line 1 collects the variables (capitals) in this constraint, using the shorthand defined. Line 2 starts by defining E, using Millman's theorem if sV is added to both sides.

From an a.c. viewpoint the upper end of u is at potential A, and so later in line 2 Millman's theorem is used to define B. If this equation is multiplied by the factor on its right it may be rewritten as (3) by using (2).

This captures D and B in terms of desired variables. It is just a little harder to do this for C. A constraint is given for it later in line 3. If the two terms in q on the right are transferred to the left hand side, the equation is justified as a statement that the current flowing away from C is just what is delivered there by Tr_2. Multiply the equation in its present form by n(s + t) as suggested on its right. It should be possible to arrive at line 4 without a pencil, using (2) and (3) to remove D and B. Collecting first the terms in A yields a coefficient uu(s + t) − un(s + t), equal to what is written. Collecting the terms in E out of B and D is easier. And the coefficient for V is simpler than expected because two terms nqs have cancelled.

Argument

The peak of difficulty is already passed, and (8) is within reach. Focus on line 1 of constraints. If the equations at the start of the next three lines were used to remove D, B and C from line 1, a gigantic equation would result. But it would only contain the desired variables E, A and V. So it would have the form of (7). If y = 0 then certainly E and A are bound into proportionality, and the sinusoid V has no effect on E, leaving it free from distortion.

You are therefore dispensed from pursuing w and x in (7): it suffices to study y alone. Now (7) is to be considered as derived from line 1 after first multiplying that line by the factor noted on its right. This suffices to prevent the generation of any fractions. So multiply line 1 as stated, and collect on its right hand side the terms in V only, including those V found when D, B and C are substituted. Hopefully this will give y as stated.

Balance equation

First note that two terms bns (h + q) cancel out in y. Now write the result line. Then divide as stated, remembering u/n = λ. But write the result in terms of impedances rather than admittances, and (8) will appear. If this holds then y = 0 in (7), and the distorting V does not influence the output.

Relation to other balances

Equation 8 now provides the balance condition for the Quad 405. It includes the driver output impedance Z_o, and the double delivery of feedback is studied. The emitter input impedance of Tr_2 is included, and the balance is altered by the new factor λ on that account.

Suppose first that this emitter input impedance is zero (λ = 1 and Z_Q = 0). Then if Z_o is also excluded by setting it infinite, (8) reduces to the balance condition of Vanderkooy and Lipshitz. But if Z_o tends to zero while g becomes large, so that gZ_o = A, the driver has become a voltage amplifier. And then (8) takes the form of (6), though Z_P is not the same because of the isolating effects of Tr_2. Of course, setting g infinite reduces (8) to the basic $Z_4/Z_1 = Z_3/Z_2$.

But none of these things are true when λ is taken into account. If the input transistor has its minimum gain of 50, then as suggested earlier $Z_T = 70\Omega$, and so λ = 0.65. Inserting this new factor disturbs all previous balance conditions. The gain of Tr_2 may rise to 300, yielding $Z_T = 15.2\Omega$ and λ = 0.90, which is still serious. It appears that the balance of the bridge is critically dependent on the gain of the particular transistor inserted at Tr_2.

Listed below (8) are approximate values, and it is clear that Z_3/Z_2 can be dismissed from the square bracket of (8). And the fractions that remain fall by about an order of magnitude a time: 1, Z_3/Z_o, k, Z_4/Z_1. It follows that for all attainable purposes the balance condition simplifies to

$$\lambda\cdot\frac{Z_4}{Z_1}=\frac{Z_3}{Z_2}+\frac{1}{gZ_p}\left[1-k+\frac{Z_3}{Z_0}\right]. \qquad (9)$$

Bridge balance

Many balance conditions have been published, but no-one has yet inserted the four Z values of Fig. 11 into their result. This may be because the simple condition $Z_4/Z_1 = Z_3/Z_2$ reduces to $L = R_1R_3C$, and it shows a 6% unbalance.

To find figures for g and Z_P in (9), consider the two 560Ω resistors in Fig. 11. These provide a nominal 50mA current sink for the dumper bases, and around crossover this current is provided by the driver. Now 1mV applied to the driver input mostly reaches the 40872 base, causing the usual 4% alteration in its collector current. This change is 2mA, which shows that the driver mutual conductance g is around 2 amps/volt. Assume minimum transistor gains, and follow the electrode impedances associated with 50mA current output back to the input terminal: the impedance there is just over 50kΩ. This is a fair figure for Z_P also, because even at 10kHz the reactance of Z_2 is still 133kΩ. So gZ_P in (9) is 10^5, or more if the transistor gains exceed minimum.

Take λ = 1 for the moment, and suppose f is the standard frequency of 13.2kHz at which Vanderkooy and Lipshitz run their tests: then the three terms of (9) work out in millionths as 498j, 468j, and 10 or less. The first two terms are imaginary and the third is real. Then the best that can be done is to balance off the first two terms by $Z_4/Z_1 = Z_3/Z_2$, and ensure that the third term is small. The designers appear to have done this. But there is still that unexplained 6% unbalance between the large terms.

But the two imaginary terms of (9) should really be balanced off by

$$\lambda\cdot\frac{Z_4}{Z_1}=\frac{Z_3}{Z_2}. \qquad (10)$$

Now the median gain of Tr_2 is 175, so its emitter input resistance may be 3300/175 + 25/6 = 23Ω, yielding λ = 0.852. The three terms in (9) now work out in millionths as 424j, 468j, and 10 or less. The first term is now some 10% down on the second, and the Quad 405 bridge appears to be out of balance by this amount in the opposite direction.

An easy way to correct this would be to reduce Z_1 by the same factor 424/468, which could be done by connecting in parallel a 4.8kΩ resistor. Now Vanderkooy and Lipshitz did vary the resistance of Z_1 to achieve minimum crossover distortion, and they demonstrate their results with oscillograms. Their finding: for best balance Z_1 requires a resistor in parallel of "about 5k". This confirms that there is a systematic unbalance of some 10% in the Quad 405 bridge, though the precise figure varies sharply with the gain of Tr_2.

Conclusion on circuit design

Clearly the dv/dt limiter R_{12} with C_6 that is causing unpredictable λ must be placed earlier in the circuit and not here. The low impedance source driving Tr_2 must be allowed direct access to this transistor, and resistors must be kept out of this area. Another way of making the same point is to observe that extra input currents flow during crossover, and the input impedance of a current dumping circuit varies wildly as a result.

There are only three terms in (9), and the third is by far the smallest at typical frequencies. If 5% components are used, as in the 405, then each of the first two terms can vary 10% by tolerance errors. Then one side of (9) may exceed the other by 20% on that account. Then it is useless to seek circuit sophistication to eliminate the unbalancing effects of k (dumper base current) in (9): any such effects are orders of magnitude less than tolerance errors. Although T. Hevreng has solved this problem in a way that must command admiration (May 1979), such a solution is not of practical utility. The correct conclusion is the inverse: k affects the balance of (9) so little that it is not worth using Darlington type dumpers to reduce it. And the Quad 405 designers were right not to bother. Equally, H. S. Malvar is not really practical in enquring after say 10% variations in g during the signal cycle.

Minor effects

Vanderkooy and Lipshitz point to the upper 560Ω resistor in Fig. 11 as an unbalancing element. It can be modelled as connected from V+D to D in Fig. 12. And a mesh-star tranformation with Z_3 and Z_4 shows that the effect is to reduce both these values by 8%, leaving unaltered the balance of the first two terms in (9). The lower 560Ω is effectively connected from D to ground, and a similar transformation with the new value of Z_4 and the load shows that this time Z_4 is effectively reduced about 1½%, but without other compensations in (9). Thus these resistors do not affect the possibility of bridge balance.

These two authors also point to the unbalancing effect of the compensation components R_{23} and C_{11} in Fig. 11. These load the driver output a little, but they can be included in the symbol Z_o of Fig. 12, so that the bridge can still be balanced. Their effect on the driver input can be seen as follows. Suppose the driver output rail in Fig. 11 is falling at 10^6V/s: then 0.33mA flows out from C_{11}, causing the top of R_{23} to fall 0.4V. If the first transistor in the driver has a collector impedance of 100kΩ when its base current is held constant, then 4μA will be drawn through it. An identical disturbance to its current would be produced by increasing its base current by 0.1μA or less. Meanwhile, in response to the driver output ramp, Z_2 is delivering 0.12mA, which is being fed to it from Tr_2. Then 0.1% increase in the value of Z_2 would increase the current in it by 0.1μA, which would come from the driver input terminal. Conclusion: the disturbance to the input can be well modelled by imagining Z_2 is increased by up to 0.1%. Compared with the tolerance error of that component this is a trivial correction.

An equivalent amplifier

Because reactive components have been used the first two terms of (9) are imaginary, and so the best that can be done to balance it is to insist on (10). But this means psu = qnt. So no V appears in the equation for C in line 4 of Fig. 12. Voltage C represents the mix of both signal and feedback, and it controls the output completely. And the equation for it is now

$$(h+q)C=-\lambda(f+p)A+\frac{m}{s+t}(\lambda p+q)E.$$

Provided that C is bound to A and E in this way any method of deriving it may be used, and will produce the same output voltage as before. For example, disconnect q in Fig. 12 and connect it in parallel with h. Then C will arise as just specified if a current equal to the expression on the right of this equation is injected into Tr_2 emitter. So replace f and p in Fig. 12 by f′ and p′, but connect the right hand side of the latter directly to E. The upper end of u may be considered to have potential. A. Then by studying only the components now connected to B it is easy to verify that the current entering Tr_2 emitter is correct if

$$p'+f'=p+f$$
$$p'=(p+q/\lambda)m/(s+t).$$

If these values are fitted the amplifier will have the same performance as the current dumping circuit. Further, Z_4 can now be shorted and its influence absorbed into V, about which we have never had to be specific. The amplifier is now shorn of its current dumping components Z_2 and Z_4, but with three others adjusted it will have identical performance.

These modifications alter the output load slightly, but that has never been a factor. Also a 520Ω load was removed from D in Fig. 12. A mesh-star transformation between this, Z_4 and Z_L shows that this removal is equivalent to increasing Z_4 by 1½%. Reduce it again and operation is as before. And the new Z_4 can be absorbed into V as previously.

The problem

In 1975 a new type of audio amplifier was announced, called the "current dumping" amplifier. Described in the US patent as "distortion-free", more than 60,000 units have now been sold, with retail value exceeding £15 million, and the design has won a Queen's Award to Industry. Yet in the lively discussion that resulted in this journal, one group insists that the amplifier works by feedforward, another school disagrees and says it uses feedback, whilst a third party maintains it is all a grave error: the performance is actually *worse* than that of a traditional circuit.

Has then *something* useful been invented, and if so exactly what is it?

A solution

Part 1, September issue, explained and simplified previous contributions in this journal. The feedforward and feedback explanations are not rivals, but valid alternatives. The bridge model developed was shown to be of greater power than the others.

Part 2 now explains the central idea of the invention, with an improved statement for the balance that must hold between the four key components in the bridge. The third party in the debate appears to be correct: the idea is spoilt by errors due to the tolerances of the components. When these are allowed for, the insertion of the current dumping components actually *degrades* the amplifier performance. Fig. 8 explains the central idea at stake.

Infertility?

Current dumping then is doing nothing useful, because of the particular bridge balance chosen. Observations of this tenor by Halliday, Olsson and Bennett were reported toward the end of Part 1, and this view is now supported by the model of Fig. 12.

Such algebra invites an explanation. The trouble seems to start with (9). Faced with that requirement a designer unsure of his g may make it large and forget it, relying on (10). And with the Quad 405 the imaginary character of the first two terms in (9) compels the designer to resort to (10).

Now redefine Z_1 in (9) as $Z_1' = Z_1/\lambda$. This means that we propose to account for the 23Ω or so impedance found at the emitter of Tr_2 by thinking of Z_1 as altered slightly to include its resisting effects. The circuit now identifies well with that of Fig. 8 with Z_1' fitted there. Now multiply (9) by Z_1'/Z_3 to yield the alternative form.

$$\frac{Z_4}{Z_3}-\frac{Z_1'}{Z_2}=\frac{Z_1'}{gZ_pZ_3}\left[1-k+\frac{Z_3}{Z_0}\right]. \qquad (11)$$

Earlier we expected the bridge ratios in Fig. 8 to be slightly out of balance if the effect of V on E was to cancel, and (11) establishes the required difference. And this difference was expected to be inversely proportional to driver gain, as it is here. But the designers have decided to neglect the gain term, found on the right of (11), and instead have set these bridge ratios equal by (10). But the entire purpose of current dumping is to define correctly the small amount by which the two bridge ratios need to be out of balance if the effects of V are to cancel. The idea is destroyed by any implementation that proposes to ignore the gain term in (11) and set these fractions equal. Such a move discards the essence of the dumping technique. And as shown above it is then possible to alter the amplifier into a conventional structure of identical performance.

Tolerances

The above criticism was based on the designer's decision to rely on (10). But further difficulties now arise, because the components he specifies to do this will not have their nominal values, but (in the Quad 405) may each be 5% out. This issue has been treated by T. C. Stancliffe (November 1976.)

The analysis in Fig. 12 will yield an accurate assessment of the effect of tolerances. Equation 8 there will not now balance exactly, but it may be made to do so with the actual components used if the left hand side is multiplied by (1 − e). We shall made no capital out of λ as a simple design improvement can remove this factor. Then e can reach 0.2 in magnitude. Prefacing the equation with (1 − e) is equivalent to asserting it with an extra leading term $-e\lambda Z_4/Z_1 = -e\lambda p/t$ instead. Then the previous equation can be asserted, with an extra leading term $-e\lambda pg'sn = -epg'su$. The previous line for y remains valid, but y is clearly now epg′su. Now multiply constraint line 1 by the factor on its right, do the elimination and verify that x in (7) is correctly stated. To verify the expression given for w, note that the last term in its first square bracket will be needed to reconcile the first term there. Examine w and x in the light of the approximate admittances listed. Dismiss the entire square bracket in w by writing out just its largest products

$$h[tu(r + kp + kl)].$$

The last of these is the largest, but it is many thousand times smaller than the last term of w, approximated by

$$w=gmpu \quad x=gu(s+t)(f+p) \quad y=epgsu.$$

Actually if all its products are multiplied out (7) contians initially 284 terms. But cancel gu in the expressions just given, and that equation reduces with great accuracy to

$$mpE=(s+t)(f+p)A+epsV.$$

The contribution to E from A may now be studied. As may be readily explained from Fig. 12 if V is held constant, there is a gain of $1 + Z_1/Z_f$, followed by an output impedance $Z_3//Z_4$.

Tolerance unbalance

Of greater interest here is the contribution to E from V:

$$E=\frac{es}{m}V\approx\frac{es}{t}V\approx e\frac{Z_4}{Z_3}V. \qquad (12)$$

This strikingly simple expression can be explained from the elementary model of Fig. 8. Consider the error in equation 8 as concentrated in Z_4: the value fitted is too large by a fraction e, because balance is achieved when (8) is multiplied by (1-e). Thus in Fig. 8 instead of the correct Z_4 the value is a fraction e larger. Once V is fixed, potentials B and D are in the merciless grip of the amplifier there. And as Z_4 is small, moving the tap at E off the balance point by eZ_4 yeilds (12).

Consider first the easy case where all components are resistive. Now V passes in almost rectangular fashion between −0.7 and 0.7V, the transition occuring during the length of each crossover. As the factors in (12) are real the distortion E given there will have the same waveform. Take e at its maximum value of 0.2 or so. Take Z_3 = 47Ω and Z_4 = 0.1Ω: the amplitude of the rectangular distortion contributed to E is given by (12) as 0.6 mV pk-pk.

Now suppose that Z_4 is inductive. As the square bracket term in (8) is small, errors in the others will dominate and e will still be real. Then it is legitimate to regard E in (12) as derived by forcing a current eV/Z_3 through this inductor, where V is a sinusoidal component of the distortion voltage. But the inductor is a linear compoent, so the various sinusoidal currents can be recomposed into a current eV/Z_3, where V now represents the full quasi-rectangular distortion voltage waveform. If L is an inductor and v is the rate of change of V this produces $E = Lev/Z_3$.

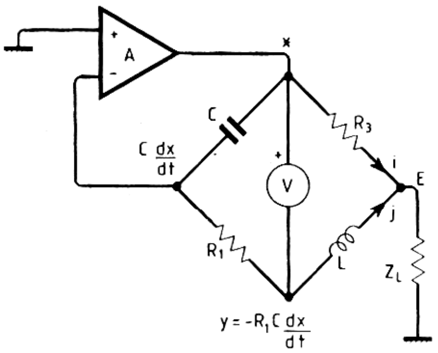
To obtain a figure for v suppose that at E the signal output is Asinωt: then near upward crossover its slew rate is Aω. To maintain this during crossover V + D has to slew an extra Z_3/Z_L times as fast (where Z_L is the load and does not refer to the inductor.) So V itself has to slew at $A\omega Z_3/Z_L$. This provides the figure for v above, yielding distortion

$$E = eA\omega L/Z_L \qquad (13)$$

constant during crossover but zero elsewhere.

Optional calculus

Calculus supports these manoevres. The argument is sketched in Fig. 13, and as investigation is concentrated on bridge unbalance the gain A has been taken as infinite. Signal has been set at zero and only the effect of V is studied. If the volts at the upper bridge vertex are x then the current through C is as stated, whence the volts at the lower vertex may be written. The two voltages must differ by V, yielding the constraint given. With the forcing function shown for V this is an easy specimen of its kind, and the full solution is sketched. As V passes the point A then x follows the broken curve shown. This may be accurately specified by saying that at A the voltage x falls by m/n, but the exponential columns shown at the origin are added back to x. At D the voltage may be said to make the same jump upward, and then to suffer the subtraction of the same columns to yield a curved transition. And y is as shown: a rectangular pulse lasting for the crossover but modified briefly at each end by the same set of exponential columns.



Constraint:

$$\frac{dx}{dt}+nx=nV, \text{ where } n=\frac{1}{R_1C}=\frac{1}{T}$$

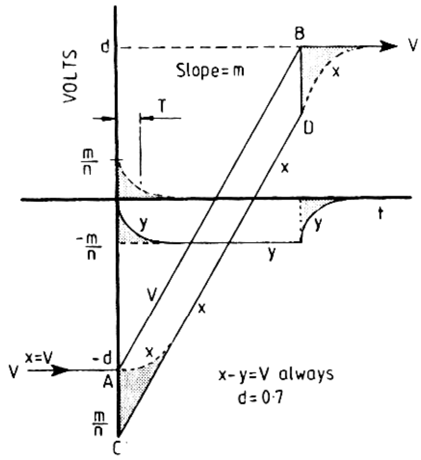


Fig. 13. With the forcing function V of slope m as drawn, x and y develop as shown. The volts y are in effect a pulse of amplitude −m/n constant during crossover but zero otherwise, as the time constant $T=R_1C\approx0.06\mu s$ only.

Rewrite (8) with $Z_1=Z_1/\lambda$ in place, to the exclusion of Z_1 and λ (the final terms in the square bracket are frivolous and may be ignored.) Now suppose the error is concentrated in Z_1'.Because for balance this equation had to be multiplied by 1 −e it follows that Z_1' is just a fraction e too small. In terms of Fig. 13 the resistor R_1 after being set at Z_1/λ turns out to have a tolerance error making it a fraction e too small.

Now suppose the change in output volts E in Fig. 12 which results from a change in V is zero. Then

$$\frac{d}{dt}(i+j)=\frac{dx}{dt}\left[\frac{1}{R_3}-\frac{R_1C}{L}\right].$$

If $R_1 = L/R_3C$ as before then i + j is constant, consistent with zero change in E, and the problem is solved. But now change R_1 to 1 − e times this expression. Examine the way in which the volts y were originally established: an additional −ey volts now appears at the lower vertex of the bridge, transmitted to Z_L/R_3 with short time constant L/R = 0.4μs. Appeal to the sketch of y: the resultant output E is a rectangular pulse of amplitude em/n for the duration of crossover. Insert for m the slew rate v derived earlier, and (13) follows. It is true that the new volts y do alter slightly the constraint given, but this is a second order effect.

Programmed model

If Z_4 in Fig. 11 is to be recognised from the start as an inductor L, then a fourth model of current dumping naturally arises. Suppose the output volts at the load are coasting steadily upward to zero from below. Then a steady voltage exists across L, with the left hand side positive. When the lower dumper goes off, the current in L has reached zero and it stays zero. There is no final spectacular rate of change to generate a transient, and all that happens is that the steady voltage just mentioned suddenly collapses. This provides the negative-going steady voltage pulse just discovered, which is applied to Z_1 and the resultant steady current integrated into a rising voltage ramp on the right of Z_2. The simplest algebra shows that if $L = R_1R_3C$ the resultant current ramp through $Z_3 = R_3$ maintains the rate of ramp of amplifier output voltage identical with its value before the lower dumper turned off.

We are left with a picture of current dumping where as crossover approaches L is programmed with a steady voltage measuring the output ramp rate. When the dumper stops conducting this programmed voltage collapses, duly executing the measures required to hold output ramp rate unaltered.

In more abstract terms L differentiates the dumper current and C recovers it by integration, together with a negative sign. As a result Z_3 passes a current equal and opposite to any sudden change in dumper current. Vanderkooy and Lipshitz make some observations on L in their article on feedforward error correction* in which they produce oscillograms to show that while a good inductor causes no trouble, an inductor wound with thick wire on a narrow former causes sharp distortion spikes during crossover, Fig. 10. The proposed explanation is that eddy currents are at work in the inductor. You might doubt whether the gentle usage just explained is apprpriate to produce such transients, and the oscillogram does resemble their Fig. 9(b), showing what happens when the bridge is unbalanced. But if this assertion is confirmed it would be a reason to expect still worse results in the first line of Table 1, reinforcing the conclusions below.

Test case

In their WW article Vanderkooy and Lipshitz provide oscillograms of crossover distortion for A = 1.4V at f = 13.2kHz with Z_L = 10Ω. When the bridge was unbalanced by reducing Z_1 by an unspecified amount, rectangular distortion pulses did indeed appear for the duration of crossover. They observed best balance when Z_1 was reduced 10%, implying an e = −0.1 for their amplifier when Z_1 is restored to its original value. Then according to (13) there should be a rectangular pulse of just 3½mV height lasting for the duration of crossover. The oscillograms

*Feedforward error correction in power amplifiers, by Vanderkoöy and Lipshitz. *Journal of the Audio Engineering Society*, January/February 1980.

(their 4c = 5a = 6a) are not easy to read, but offer 4mV pk-pk amplitude. The pulse appears to be rectangular, but to include as well perhaps a 60% overshoot on return. The overshoot then decays with time constant about 5μs. All this is encouraging, and can be made more so.

Taking median gain figures for the transistors in the driver, its input impedance would be 460kΩ, combining with C = 120pF to yield 55μs time constant. This is not likely to be the decay involved. But C_6 with R_{12} yields 3.3μs, or slightly more if the source driving V_{in} offers some impedance at r.f.

With the output described, crossover lasts 2.2μs, as seen in Fig. 11 from the effect on output of 1.4V transition at the driver output. Then initially C_6 offers a short circuit to ground for the rectangular pulse offered to it via Z_1 and Tr_2. But as the pulse developes it begins to compare with 3.3μs. Then C_6 has largely charged, and the pulse faces almost R_{12} instead of a short to ground. And when the pulse has finished C_6 has to discharge. It forces reverse current into Tr_2 and causes the overshoot noticed, which then decays as it should with time constant 4 to 5μs. The oscillogram provided is now well explained.

If the experiment were repeated with larger A, then crossover time would fall in proportion, and C_6 would not have time to develop significant charge. The circuit would tend to behave more as if R_{12} were shorted. Thus as A rises in this way the circuit moves from something like 10% unbalance in one direction, passing zero to arrive at 6% unbalance in the other.

These figures were justified earlier. Then as A rises in (13) the quantity e first falls towards zero and then rises on the other side. So initially not much increase in output distortion is expected, as these factors are behaving in opposition. But after a while distortion should rise rapidly, perhaps after the style of a square law, when both factors are pulling in the same direction. This is just what is reported: as A was increased up to 14V there was little increase in distortion, but as A climbed by a further factor of 2.5 distortion rose by a factor of five (observe approximate square law behaviour!)

Further progress would require more and clearer oscillograms.

Traditional amplifier

How does crossover distortion in the circuit of Fig. 11 compare with that present in an equivalent traditional amplifier? Some comparisons have been based on shorting Z_4 while leaving Z_2 in place but these need not detain us. It is clear that the capacitor Z_2 will then seriously inhibit the driver in its attempts to produce rapid transition of its output voltage during crossover. Hence no traditional amplifier would contain such a component.

A comparison was made above with a traditional amplifier, and it was found that there was no difference. But this supposed a dumping amplifier that had been perfectly balanced by (10). Now compare a dumping amplifier with unbalance leading to (13) with a traditional amplifier, and figures become essential.

The circuit of Fig. 11 may be converted into the equivalent traditional amplifier by shorting Z_4, and also removing Z_2. further, R_{12} should be shorted and C_6 removed: impedance cannot be tolerated in this area, and dv/dt limiting must be done earlier instead. Copy the circuit of Fig. 12 with these simplications.

Then D becomes equal to E, and if study is confined to the effects of V on E then C becomes just a multiple of E. As Tr_2 emitter input impedance is now low B can be taken as zero and all three unknown voltages that previously had to be eliminated have now vanished. The problem can be solved in two lines by applying the same current constraint as previously, and the contribution to E due to V becomes

$$E \approx -\frac{1}{gZ_{in}} \cdot \frac{Z_1}{Z_3} V.$$

As all components are resistive, E will just follow the waveform of V in this fashion. The worst figure of 50kΩ for Z_{in} produces 0.15mV pk-pk to complete Table 1.

Results

Current dumping has aroused much interest, and there have now been some 20 contributions to the discussion in this periodical alone. It has been suggested here that when the analysis takes account of the delivery of feedback to both ends of Tr_2 a new factor λ appears in the bridge balance (9). The new factor is due to the presence of R_{12} and may vary between 0.65 and 0.90 depending on the gain of Tr_2. Supposing that this gain has its median value it would appear that a 10% bridge unbalance is built into the design of the Quad 405. This result has been accurately verified by Vanderkooy and Lipshitz. Conclusion: R_{12} is causing unpredictable consequences and it must go. The bridge must be balanced.

But suppose this is accepted (or indeed rejected). Then the best attempt at bridge balance is to ensure that (10) holds. But this destroys the whole system, and an amplifier of traditional type and identical performance results if the dumping components Z_2 and Z_4 are removed, provided three other elements are adjusted.

Finally, tolerance errors prevent perfect balance of (10), and further distortion results, degrading the current dumping amplifier below its traditional equivalent. Final figures are in Table 1. It seems to be an improvement to use resistive rather than reactive dumping elements, and a further improvement to abandon them altogether.

The gain term in (9) is about 10^{-5} in the Quad 405, and it will almost certainly be small in any implementation of current dumping. Given the tolerances of the other terms it will scarcely be possible to take it into account. Then objections would apply unaltered to any alternative dumping circuit.

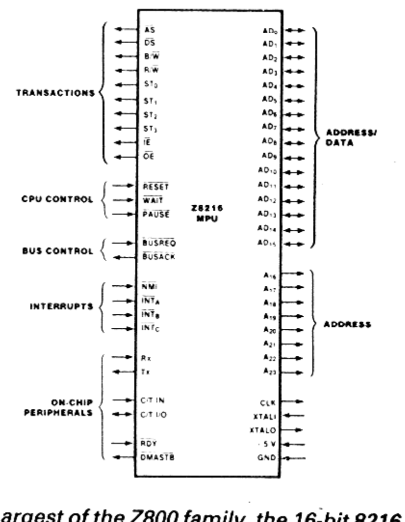
Part 1. On page 43 of the September article, the lower Z_4 in equation 5 should read Z_1. WW

The new Z80

Coinciding with the introduction of the 32-bit Z80000 mid next year Zilog plan to introduce the Z800 8/16-bit family of processors with Z80 software compatibility. With clock rates of up to 25MHz (preliminary information) and memory manipulation features, these devices will also make full use of current high-speed rams and, besides providing a stop-gap for the eight-to-sixteen bit transition, the family will act as input/output processors for the 16-bit Z8000. There are four devices: two with a 16-bit data bus, the Z8116 and 8216; and two with eight bits, the Z8108 and 8208. The 82 versions are physically larger than the other two i.cs and have four direct-memory access channels and built-in uart: all of the i.cs have four 16-bit counter timers.

The new processors have an integral memory-management unit that allows them to access either 512K-bytes or 16M-bytes, depending on the type, and they have 256 bytes of memory which, when configured as a 'cache', may be programmed to contain either instructions or data, or both. This speeds up program execution by reducing the number of external bus accesses. Operation and updating of the cache is automatic.

Although the instruction set will be expanded and augmented, all Z80 instructions are compatible with binary. Basic addressing modes of the Z80 will be augmented with the addition of a base-index mode and 16-bit displacements for indexed, program-counter-relative and stack-pointer-relative modes. These new addressing modes are incorporated into many of the old Z80 instructions. Additions to the instruction set include 8/16-bit signed and unsigned multiply and divide, 8/16-bit sign extension, and a test-and-set instruction for use in multi-processor applications. Sixteen-bit instructions include compare, memory increment/decrement, negate, add, and subtract.



Largest of the Z800 family, the 16-bit 8216, with Z80 instruction compatibility. Of the four devices, the two eigth-bit versions are compatible with the Z80 bus and the two 16-bit versions are designed for use with the 16-bit Z-Bus.

WW314 for further information