LOW-DISTORTION STEREO DECODER

John Linsley Hood brings you a practical FM receiver design which uses some of the techniques described in his recent theoretical series. To begin with here's the stereo decoder board.

The stereo decoder circuit presented here has been designed to enable the highest practicable audio quality to be obtained from a good FM tuner. In particular, the audio signal path has been kept entirely separate from the 38kHz switching circuitry and uses discrete components rather than ICs. The results include a total harmonic distortion figure of 0.02% over the entire VHF/FM signal bandwidth (30Hz–15kHz) in both mono and stereo modes, more than 20dB attenuation of the 19kHz pilot tone and over 60dB attenuation of the 38kHz switching waveform.

These figures are reflected in the overall sound quality provided by the decoder when used in conjunction with a good quality FM tuner. The stereo image position and stereo separation are particularly good. Because of this, the decoder should prove of interest both to those who are building an FM receiver from scratch and those who already have a receiver and wish to upgrade it.

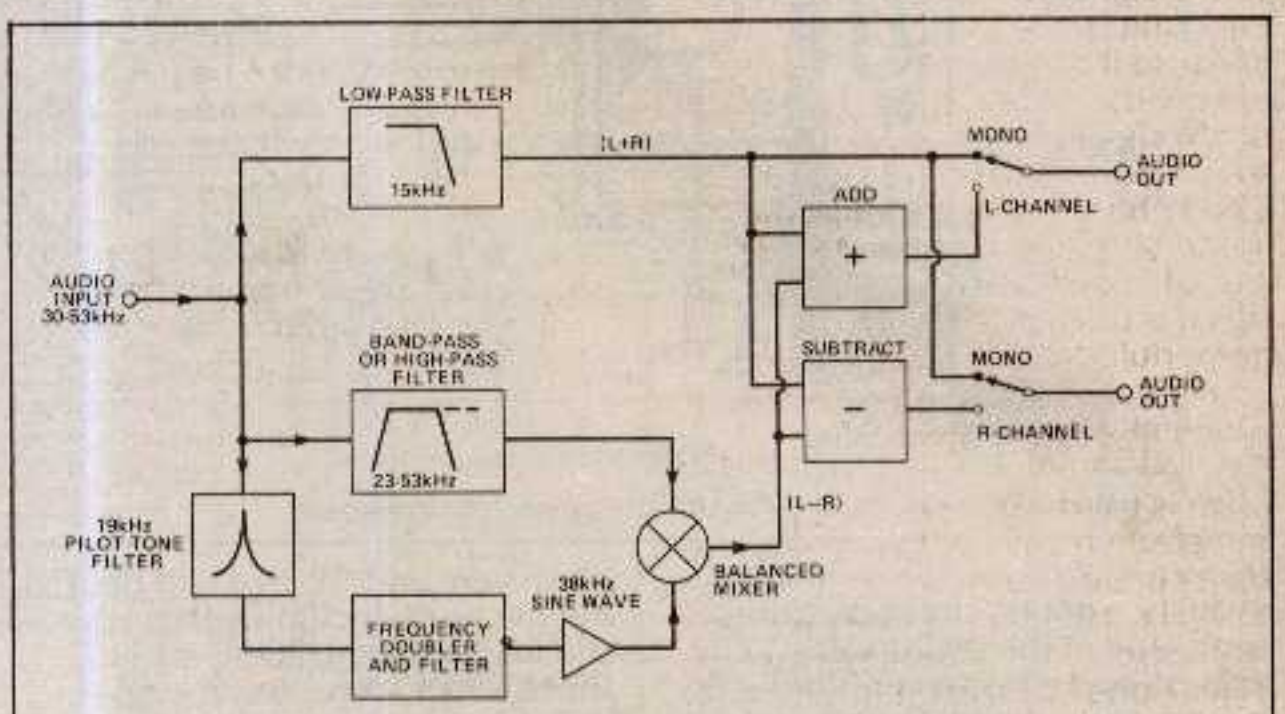

Fig. 1 A matrix-type stereo decoder.

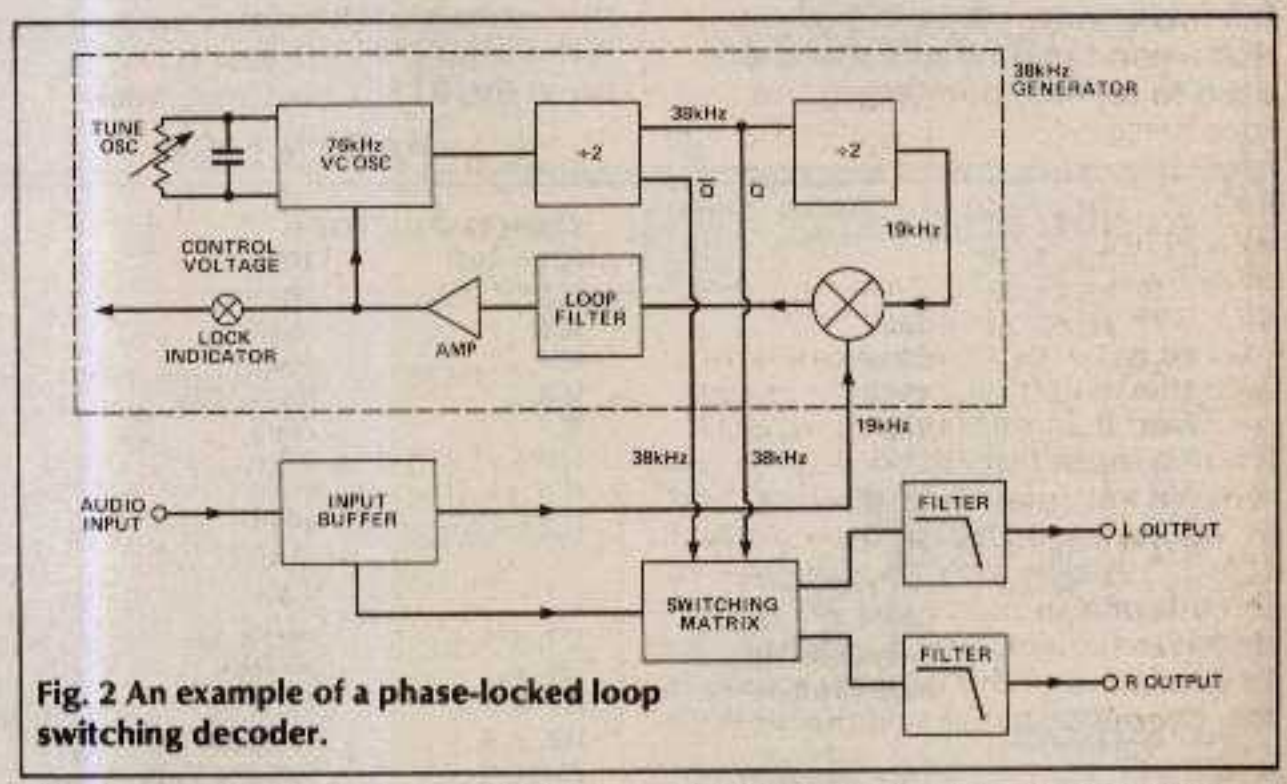

Fig. 2 An example of a phase-locked loop switching decoder.

Stereo Decoding

One of the major advantages of VHF FM radio broadcasting is that the available bandwidth is adequate to allow the transmission of a stereo signal. This is done using the Zenith-GE pilot tone system as described earlier in this series of articles.

The advantage of this method is that the signal is broadcast as a composite. The normal 20Hz–15kHz part of the audio modulation is a perfectly conventional mono (left plus right) transmission, while the necessary additional information required to generate two separate channels is carried as a normally-inaudible suppressed carrier, centred on 38kHz and occupying the 23kHz–53kHz part of the AF spectrum.

There are two basic methods of recovering the stereo information from this composite signal (Figs. 1 and 2). The first of these uses the 19kHz pilot tone to regenerate a 38kHz carrier so that the sidebands can be recovered from the 23–53kHz signal in the normal way. The second method uses a switching system operating at 38kHz, to alternately route the whole signal to the left or the right channel outputs.

Both of these methods effectively do the same thing, but there are differences in the

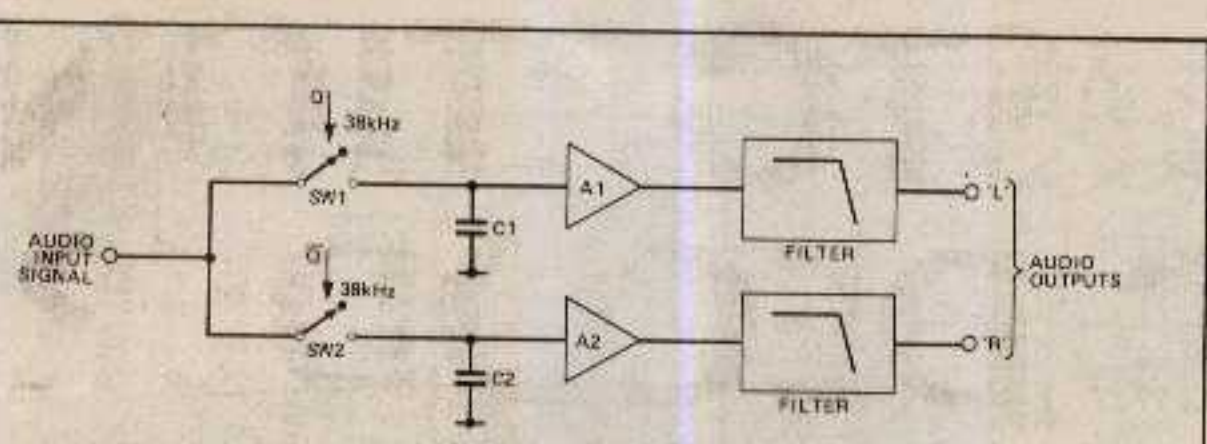

Fig 3. Block diagram of a sample-and-hold signal splitting circuit.

potential signal-to-noise ratio which relate particularly to the effective bandwidth of the decoded signal.

The signal-to-noise ratio of the stereo signal will always be worse than that of the mono signal because it requires more bandwidth. While the magnitude of the signals is the same, the stereo one demands at least a 53kHz bandwidth whereas the mono one only requires 15kHz, and the noise associated with any signal is related to the demodulation bandwidth needed.

However, there is an additional problem with the switching method shown in Fig. 2. If a square wave is used as the switching waveform it will contain a whole series of odd harmonics, at 114kHz, 190kHz, 266kHz etc, and any noise components lying within 19kHz on either side of these will also be commutated down into the audio band.

The matrix system of Fig. 1 is free from this problem — provided that a good quality sine wave is used to replace the 38kHz suppressed carrier. To generate a good sine wave which is accurately locked in phase to the 19kHz pilot tone is not easy, and any error in phase will substantially impair the effective channel separation.

The noise problems associated with the switching decoder can be removed if an effective bandwidth limiting input filter is used to remove any incoming noise signal in the frequency band from 95kHz (38x3–19) upwards. This allows the use of a simpler type of decoder system, which can be built in a form which offers a very low overall distortion of the audio signal.

The Sample And Hold System

Two further requirements of any decoder system, in addition to low noise and low distortion, are that the audio signal output level shall be identical in both mono and stereo modes, and that it is possible to switch from one to the other noiselessly. Both of these additional requirements are met by the sample and hold arrangement shown in Fig. 3.

In the mono mode, when both SW1 and SW2 are closed, it is evident that the same signal is being fed to both the left and right channels. If the switches are sequentially operated, the holding action of capacitors C1 and C2 will result in an output signal which is identical in amplitude to the incoming one, apart from any

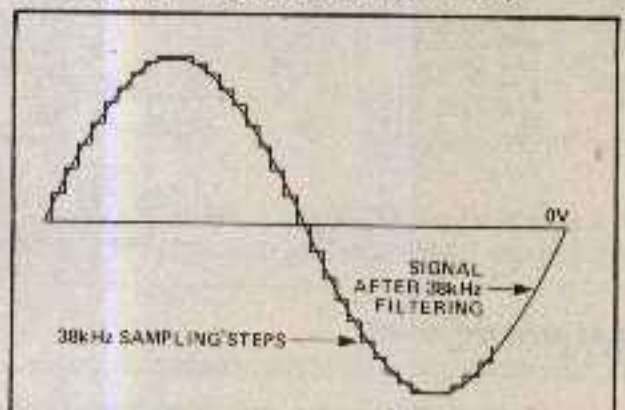

Fig. 4 The sort of waveform produced by a sample-and-hold circuit.

differences in the left and right signals. This is illustrated for a single channel in Fig. 4.

The requirements for correct operation of this circuit are that the switching action should take place at the correct time in relation to the incoming signal waveform, that the time required to charge C1 and C2 from the source through the switching shall be very small in relation to the switching time, and that the discharge time through the input impedances of A1 and A2 shall be very long in relation to the sample period.

In this circuit, Q1 and Q2 form a third-order active low-pass filter. However, only two of the necessary low-pass RC elements are present on the decoder board since the third (5.7us) component was provided by the PLL loop characteristics of the circuit with which it was designed to be used.

Where this decoder is used with a demodulator without AF output low-pass filtering, it is necessary to add the network R41/C27. With the PLL tuner described in the following part of the article, this is switchable to give a wide or narrow effective bandwidth. Where the signal strength is good, leaving SW2 open gives a slightly better image separation. With it closed, the signal-to-noise ratio is improved by about 6dB with only a small loss of stereo width.

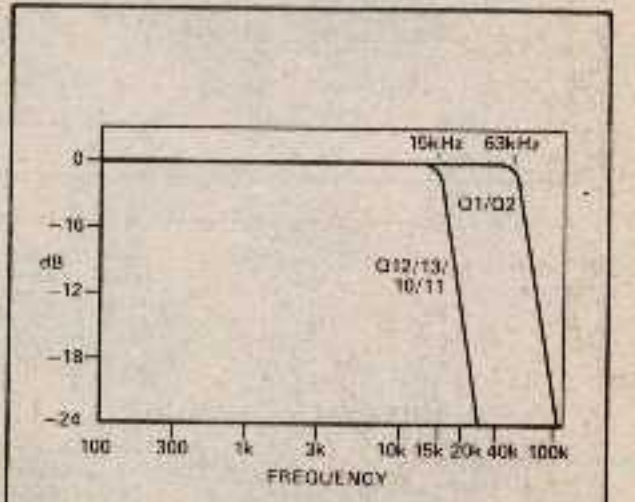

Fig. 5 Transmission characteristics of the input and output filters used in this design.

A similar filter is used after the sample-and-hold switching FETs (Q8, Q9) to produce a rapid attenuation beyond 16kHz. By leaving the 75us de-emphasis network to follow it, the required attenuation of the 38kHz switching waveform ripple is still further increased. The attenuation characteristics of the input and output filter circuits are shown in Fig. 5.

The Switching Waveform Circuit

The 38kHz switching waveform used to drive the FET switches is derived from a standard 1310-type PLL stereo decoder, IC1, which is employed to monitor the incoming signal and extract the 19kHz pilot tone when present.

When the 19kHz pilot tone is present, a 76kHz sawtooth will appear at pin 14 of the phase-locked loop, locked in period to the pilot tone. A DC signal will also be present on pin 6, and can be used to actuate an indicator LED when the 19kHz pilot tone is detected. This DC signal is also used in the circuit shown in Fig. 6 to operate a DC switching transistor, Q4, which controls the supply to IC2. This is a CMOS dual D-type flip-flop, which is used to generate the symmetrical 38kHz switching signal.

In the absence of a DC output current from pin 6 of IC1, Q4 is

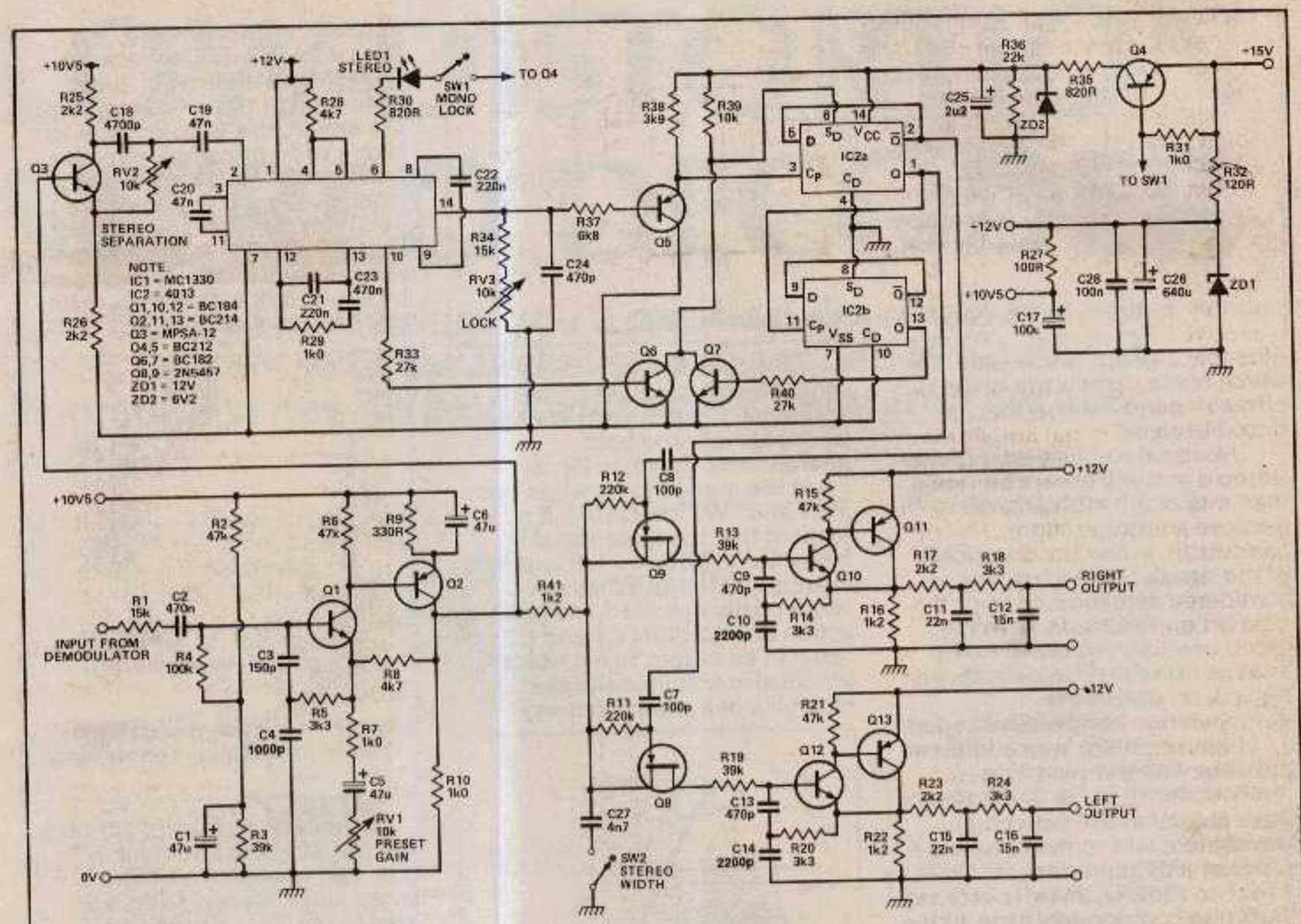

Fig. 6 Complete circuit diagram of the FM stereo decoder.

non-conducting, IC2 is inoperative, and both of the switching FETs (Q8 and Q9) are permanently conducting. The incoming signal from the demodulator will thus be passed directly to both the left and right output channels without interference from the switching/decoding circuitry. Opening switch SW1 will maintain this condition even when a stereo signal is present.

BUYLINES

A complete kit of parts for the FM stereo receiver will be available from Hart Electronic Kits, Penylan Mill, Oswestry, Shropshire SY10 9AF. They will be supplying parts for both the decoder and the other sections of the receiver which have yet to be published, and they will happily provide individual components or part kits as well as full kits. Prices had yet to be finalised at the time of going to press, so intending constructors should contact Hart on (0691) 652 894. The PCBs will be included in the kits, and since Hart will supply these separately too we will not be offering them through our PCB Service.

Provided that a stereo signal is present and the PLL IC has been correctly tuned, a 76kHz sawtooth waveform will be fed to Q5 and to IC2 as a clock signal. The first divide-by-two output signal pair in IC2 produces a 38kHz signal from this clock and drives Q8 and Q9.

Unfortunately, it would be possible if the circuit were switched off for the left and right channels to be reversed, since their identity depends on the relative phase of the 38kHz waveform. This possibility is removed by using the second-stage (19kHz) output from IC2 to feed a simple two-transistor NOR gate, Q6/Q7. The other input to the gate is taken from the 19kHz output of the 1310. If these should become synchronous in phase, the collectors of Q6, Q7 will rise toward the positive rail and reset IC2 for one half cycle, restoring the correct switching phase.

Because of the sample and hold action of the decoder, the stereo/mono transition is completely noiseless.

The best separation between the two stereo channels is given when the phase of the 38kHz switching waveform is timed precisely to coincide with the L-R channel transisitons at the transmitting station encoder, from which the 19kHz pilot tone is derived.

Since, in this circuit, the audio channel and the switching waveform channels are handled separately, it is possible to feed the 19kHz pilot tone through a phase-angle adjusting all-pass filter, Q3. This allows the phase of the pilot tone fed to the PLL (IC1) to be adjusted to give the greatest L–R separation. The adjustment is provided by RV2.

Construction

The majority of the components for the stereo decoder are mounted on a single-sided PCB. The only exceptions are the panel-mounting components (LED1, SW1, SW2, etc) and the second stage of filtering on the two outputs (R18/C12 and R24/C16).

Begin assembling the board by installing the four wire links (all around Q4 and IC2) and the IC