THE PRACTICAL USE OF CURRENT DUMPING FOR HIGH POWER AMPLIFIERS

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J. Celen and W. Sansen.
ESAT, Elektrotechniek
Katholieke Universiteit Leuven
Kardinaal Mercierlaan 94,
B 3030 Leuven, Belgium

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ABSTRACTS

The theoretical aspects of current dumping are discussed. An example of a high power amplifier has been built with very cheap and slow output transistors. It uses a class-G configuration to increase the efficiency and has no quiescent current. As a consequence the power block introduces a lot of distortion. Yet the distortion of the whole amplifier is very low.
Its characteristics are : an output power of 500 W in a load of 8 ohm, a slew rate of 25 V/ μs, a high power bandwidth of 32 kHz and a harmonique distortion of 0.0024% at 500 W 1000 Hz.

Introduction

The current dumping principle takes advantage of the combination of feedback and feedforward to reduce distortion in audio amplifiers. Much has been written about this principle and yet at present there is only one commercial current dumping audio amplifier on the market.
The first paragraph gives an overview of the origin of the current dumping principle. It explains how it must be considered as a combination of feedback and feedforward. Also a physical explanation is given.
In the second paragraph we discuss the relationship between the power block and the correction amplifier. A relationship between their output currents, gain bandwidth products and slew-rates is derived and discussed. Three different ways of implementation are presented and discussed.
The third paragraph describes a prototype of a 500 W amplifier based on the configuration with the lowest distortion. The power block uses four different power supplies. This class-G configuration has a higher efficiency than the class-B principle. There is no quiescent current in this section.

As a consequence this section cannot give any thermal problem. This section gives a lot of distortion and yet at the output of the amplifier all of the distortion is totally cancelled.
The correction amplifier can deliver 120 mA and has a gain bandwidth product of 200 MHz. By adding a second powerblock, the amplifier can be modified to deliver 1000 W in a 4 ohm load.

1. Origin of the current dumping principle

1.1. Error feedforward.

With the error feedforward technique it is possible to reduce the distortion of an amplifier by application of a finite amount of feedforward without the necessity of reducing the amount of feedforward at higher frequencies. This means that the feedforward is free from all types of distortion over a wide frequency range. Let us look how it works.

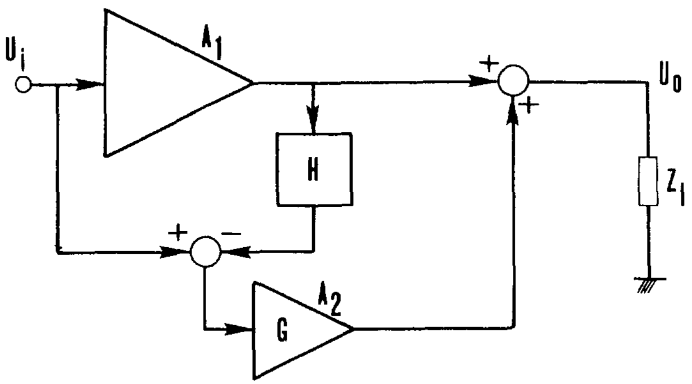


Fig. 1 : The feedforward configuration.

In fig. 1, the attenuated output of the power amplifier A_1 is substracted from the input signal and this difference is amplified by the correction amplifier A_2. The correction power is summed with the power of the head amplifier to produce the output signal of the whole amplifier. It is easy to calculate that the output signal of the amplifier is free of the errors due to A_1 if G.H equals unity. This configuration does not use any feedback loop and consequently there are no stability problems.
The problem of this configuration is the omission of a true biconjugate output summing network. A solution for this problem is given in fig. 2.

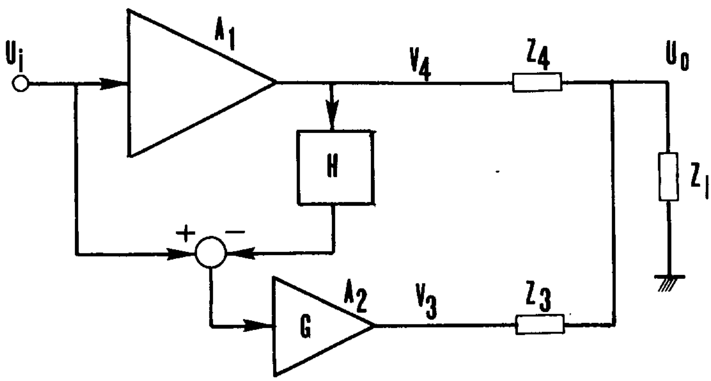


Fig. 2 : A practical realisation of the output network.

If we make $$G.H = \frac{Z_3}{Z_4} \tag{1}$$

then the transfertfunction of fig. 2 is :

$$\frac{u_o}{u_i} = \frac{Z_1 Z_3}{Z_3Z_4 + Z_4Z_1 + Z_1Z_3} \cdot \frac{1}{H} \tag{2}$$

If Z_4 and Z_3 are small in comparison with Z_1 then we can say that

$$\frac{u_o}{u_i} \approx \frac{Z_1}{Z_1 + Z_3//Z_4} \cdot \frac{1}{H} \qquad (3)$$

Equation 3 shows us that we have an amplifier with a gain $\frac{1}{H}$ and an output impedance equal to the parallel of Z_3 and Z_4.

1.2. Current dumping.

In fig. 2 we want that the amplifier A_2 should deliver only a small portion of the output power. This power is meant to correct the errors due to A_1. In practice it would be logical to choose Z_4 small relative to Z_1 and Z_3 should be greater than Z_4. As the correction amplifier will correct every error of A_1, the head amplifier A_1 can derive its input from any convenient signal. This may be interesting if we want to reduce the load on A_2. In fig. 3 we have derived the input of the head amplifier from the output of the correction amplifier. Suppose that the head amplifier is a unity gain source follower. This arrangement ensures now automatically that the output signal of the correction amplifier is as close as possible to the desired output signal which leads to a minimum output current of the correction amplifier.

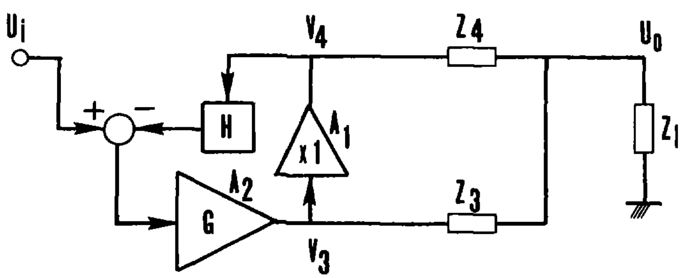


Fig. 3 : The current dumping configuration.

By connecting the output of the correction amplifier to the input of the power block, one of the most interesting properties of the feedforward principle has been cancelled. We have a loop G ; A_1; H which might lead to oscillations.

The transfertfunction of this configuration is given by (2).
Regarding this expression one might conclude that the power block is of no importance to the stability of the whole amplifier. In practical realisations it is difficult to satisty the condition (1) especially at high frequencies. To avoid oscillations the loop G A_1 H should have a gain as is indicated in fig. 4. In this figure ω_2 is the first pole of the power block.

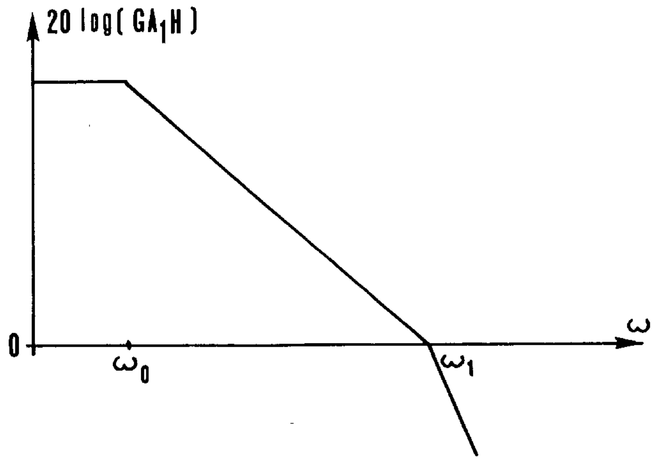


Fig. 4 : Gain of the loop G A_1 H.

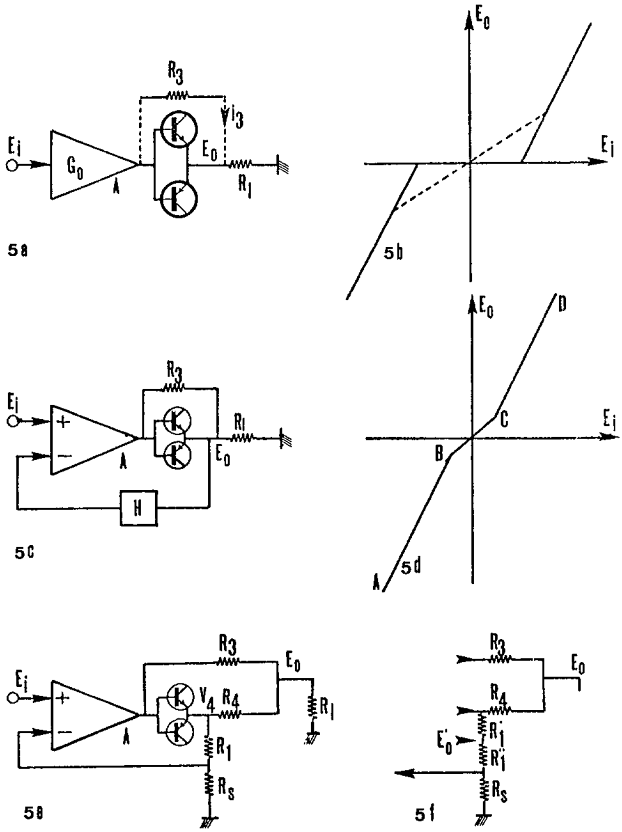
One can conclude that G.H should have an integrating characteristic.

$$G.H = \frac{A_o}{1 + s\,\tau_o} \tag{4}$$

As $\frac{Z_3}{Z_4}$ must be equal to G.H, Z_3 can be a resistor and Z_4 an inductor in series with a resistor.

1.3. Physical explanation of the current dumping principle.

Consider fig. 5a in which A is an ideal amplifier, followed by two transistors whose bases are connected together. The transfer characteristic of this amplifier for a resistive load will be as given in fig. 5b, causing a lot of distortion. This characteristic can be improved by bridging the output transistors by a resistor R_3 as is done in fig. 5a. A feedforward current I_3 is supplied by R_3 to correct errors in the region near $E_o = 0$.
A second improvement is found in the application of feedback. If $H = \frac{1}{G_o}$ then we have the characteristic of fig. 5d. But how much feedback we apply, It can never be perfect. To obtain a perfectly linear line, there should be a little more negative feedback in the regions AB and CD (fig. 5d) where the output transistors are on, than in the region BC where the dumpers are off. This can be done by inserting a resistor R_4 between the output transistors and the load (fig. 5e).



When the circuit of fig. 5d is handling a low level signal, the output transistors are off. The voltage V_4 is equal to E_o and the feedback is $R_s/(R_s + R_1)$.
For a high level signal the output dumpers are on and a current I_4 flows through R_4. V_4 is now different from E_o. Immagine now that we replace R_1 by two resistors R_1' and R_1'' so that $E'_o = E_o$, (fig. 5f), and $R_1' + R_1'' = R_1$.

As now $E_o' = E_o$ is, we can conclude that tne feedback is now $R_s/(R_s + R_1'')$.
As $R_1'' < R_1$, the feedback is now greater than in the case where the output transistors are off.
By means of a correct choice between the resistors and the gain of A, it is possible to make the transfert characteristic perfect linear without the need for an infinite gain nor infinite feedback.

2. The correction amplifier.

2.1 The feedforward current.

2.1.1.

Let us determine the amount of output current in the correction amplifier. We want the error correction current to be as low as possible because too much feedforward current leads to high dissipation and distortion in the error correction amplifier itself.

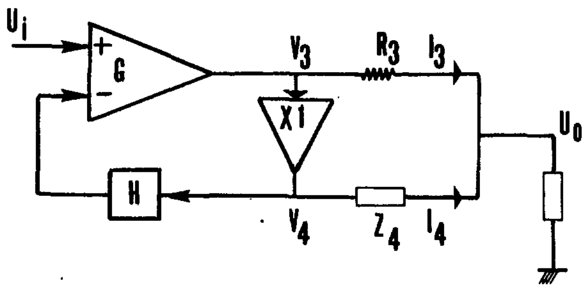


Fig. 6 : The calculation of the feedforward current.

If we suppose that the power black has an infinite input impedance, then the current of the correction amplifier is :

$$I_3 = \frac{V_3 - u_o}{R_3} = \frac{V_\delta}{R_3} + \frac{I_4 . Z_4}{R_3}$$
$$= \frac{V_\delta}{R_3} + \frac{I_4}{GH} \qquad (5)$$

We see that this current consists of two components. We have one portion to correct the errors of the power block and a second part which is proportional to the output current of the power block.

How can we take care of a minimum load on the correction amplifier ?

1. Try to have the distortion of the power block to be as low as possible.
2. Try to have the input impedance of the power block to be as high as possible.
3. Equation 5 indicates that I_3 will be less as R_3 increases. But when we increase R_3 we will have to increase Z_4 as well as $\frac{R_3}{Z_4}$ must be equal to G.H. Increasing R_3 and Z_4 leads to a higher output impedance which is not desirable.
4. Equation 5 indicates too that I_3 decreases when the loop amplification G.H increases. But increasing G.H leads to a higher gain bandwidth product of the correction amplifier which is given prone to oscillations.

A practical formula to calculate the maximum current I_3 can be as follows :

$$I_3 = \frac{V_\delta}{R_3} + \sqrt{\frac{2P}{R_L}} \cdot \frac{\sqrt{\omega_M^2 L_4^2 + R_4^2}}{R_3} \qquad (6)$$

where : P : output power of the amplifier

R_L: load of the amplifier

$\omega_M = 2 \pi f_m$

f_m: power bandwidth of the amplifier.

2.1.2.

Due to the presence of the inductance L_4, there is a limitation on the slew rate of the amplifier. Indeed, the output current of the correction amplifier is limited. This has as a consequence a limitation on the maximum voltage on the inductor L_4. For an inductor we have that $V_{L_4} = L_4 . \frac{dI}{dt}$. We see now that there is a slew rate on the output voltage of the amplifier due to the presence of the inductor and the limitation of the current of the correction amplifier.

For a resistive load the slew rate is :

$$S.R. = \frac{dV}{dt} = R_L \cdot \frac{dI}{dt} = R_L \; \frac{I_{3_{max}} \cdot R_3 - V_\delta}{L_4}$$

If one wants to build a very fast amplifier it is good to take L_4 as small as possible. Slow output devices can be used giving a large ' which then must be compensated with a large current I_3. Note that the use of very fast output transistors is not sufficient for a high slew rate.

2.2. Design of the correction amplifier.

Let us now examine how we can build an amplifier corresponding to fig. 7 so that the condition $G.H = \frac{Z_3}{Z_4}$ is satisfied.

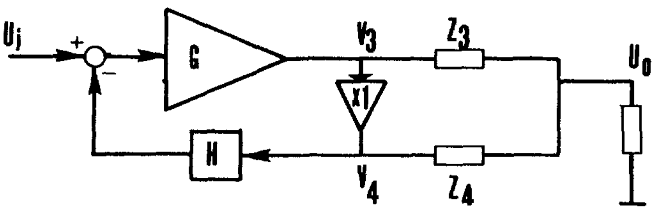


Fig. 7 : $V_3 = G(V_i - H\,V_4)$ (7)

$$GH = \frac{Z_3}{Z_4}$$

$$\frac{U_o}{U_i} = \frac{Z_L}{Z_L + Z_3//Z_4} \cdot \frac{1}{H}$$

2.2.1. The first configuration that will be described is the one used in the quad. 405.

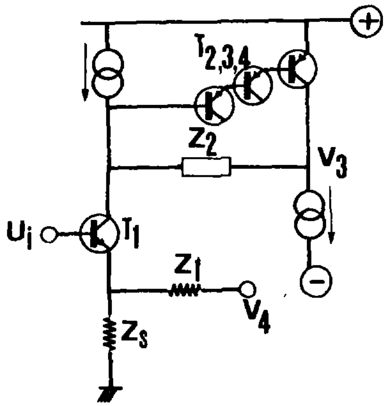


Fig. 8 : Block scheme of the correction amplifier of the Quad 405.

In fig. 8, the transistors T_2, T_3 and T_4 form an amplifier with very high input impedance and high amplification. This has as a consequence that all of the a.c. current, provided by the summarizing transistor T_1, flows into the impedance Z_2. The transductance g_m of T_1 is stabilized by the current source. Replacing T_1 by a simplified hybride π model we can calculate V_3 as a function of u_1 and V_4 (fig. 9).

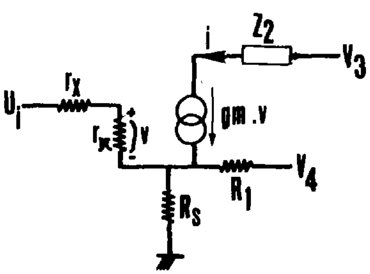


Fig. 9 : A small signal model of fig. 8.

$$g_m.v = \frac{U_1}{\frac{1}{g_m} + R_s//R_1} - g_m \cdot V_4 \cdot \frac{\frac{1}{g_m}//R_s}{\frac{1}{g_m}//R_s + R_1}$$

If $\frac{1}{g_m} \ll R_s < R_1$ then we can say that

$$g_m . v = V_i \frac{R_s + R_1}{R_s \cdot R_1} - V_4 \cdot \frac{1}{R_1}$$

and that

$$V_3 = i \cdot Z_2 = V_i \left(\frac{R_s + R_1}{R_s \cdot R_1} \right) Z_2 - V_4 \cdot \frac{Z_2}{R_1} \tag{8}$$

Comparing (7) and (8) we find that

$$G.H = \frac{Z_2}{R_1} \quad \text{and} \quad H = \frac{R_s}{R_s + R_1}$$

The requirement for zero distortion from the output transistors is now :

$$G.H = \frac{Z_2}{R_1} = \frac{R_3}{Z_4} \tag{9}$$

When $Z_4 = L_4$, then Z_2 must be a capacitor so that $L_4 = R_3 R_1 C_2$.
But when the four impedances satisfie exactly to equation 9, it is not possible to chancel all the distortion of the output block. The loop amplification G.H is not exactly equal to $\frac{Z_3}{Z_4}$ due to the simplification we have made.
It is important to have a large D.C. current in the input transistors to provide for a great transductance. A large D.C. current is also interesting to provide for a high slew rate of the correction amplifier.

2.2.2.

A better solution to avoid the distortion produced by the input summing transistor can be the use of a differential pair. A configuration is given in fig. 10.

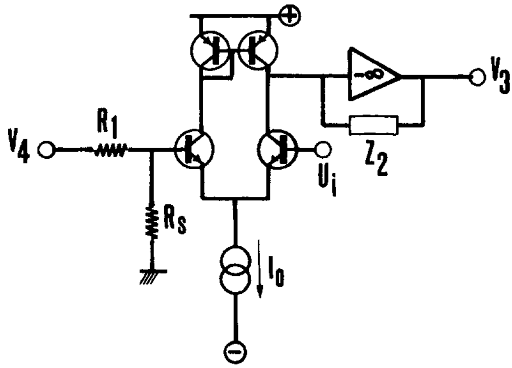


Fig. 10 :

If one uses input transistors with very high β, then V_3 is :

$$V_3 = Z_2 \cdot 38\ I_o (V_i - \frac{R_s}{R_1 + R_s} V_4)$$

In this case the loop amplification is :

$$GH = Z_2\ 38\ I_o \cdot \frac{R_s}{R_1 + R_s} = \frac{Z_3}{Z_4} \qquad (10)$$

The slew rate is :

$$S.R = \frac{I_o}{C_2} = \frac{1}{38} \cdot \frac{1}{H} \cdot \frac{R_3}{L_4} \qquad (11)$$

We see that the correction amplifier will be faster when $\frac{1}{H}$, the amplification of the whole amplifier, will be higher and when the gain bandwidth product of the loop G.H, will be higher.
Increasing the first one gives no problems but increasing the last one can lead to oscillations.

2.2.3.

In the preceding shemes, a part of the loop gain is stabilised by the impedance Z_2. But there is no stabilisation on the whole loop. A better solution is found in fig. 11.

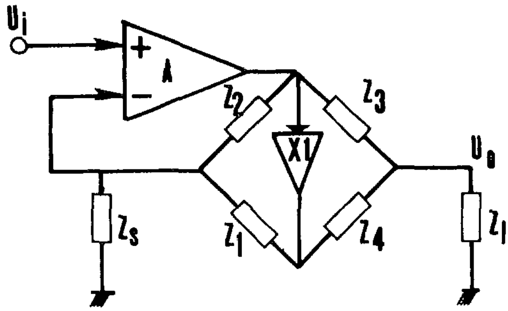


Fig. 11 : The gain of the loop is now stabilised by the impedances Z_2 and Z_1.

If we use a singelpole compensated correction amplifier with an infinite input impedance, and zero output impedance and a gain :

$$A = \frac{A_o}{1 + s\tau}$$

and $Z_3 = R_3$

$Z_4 = R_4 + j\omega L_4$

$Z_1 = R_1$

$Z_s = R_s$

$Z_2 = R_2' + R_2 // C_2$

then the conditions to have $G.H = \frac{Z_3}{Z_4}$ are :

$$A_o = \frac{R_2}{R_2'} = \frac{R_3 \cdot R_1}{R_4 (R_2' // R_1 / R_s)} \tag{12}$$

$$\tau = \frac{L_4}{R_4} = C_2 \; R_2 \tag{13}$$

It is important to note that A must always be greater then $\frac{Z_3}{Z_4} \times \frac{1}{H}$.
Remark that the gain bandwidth product of the amplifier is

$$\omega_A = A_o \cdot \frac{1}{\tau} = \frac{1}{R_2' \; C_2} \tag{14}$$

It follows that $\omega_A > \frac{R_3}{L_4} \cdot \frac{R_1 + R_s}{R_s}$ (15)

We have supposed that the output impedance of the correction amplifier be zero. In reality this is impossible. A solution for this problem is found in ref. 2. But in realistic circuit Z_o can be made small and the input impedance of the power block high. The error can then be neglected.

3. Actual realisation of a current dumping amplifier and measurement results

A 500W current dumping audio amplifier has been built according to the principles explained in 2.2.3. The components of the bridge have values :

R_1 = 1000 ohm
R_2' = 4,7 Kohm
R_2 = 4,7 Mohm   adjustable
C_2 = 60 pF
R_3 = 100 ohm
R_4 = 0,033 ohm
L_4 = 3.9 μH
R_s = 100 ohm

The maximum output current of the correction amplifier can be calculated using (6) giving 120 mA. (We want 500W into 8 ohm with a power bandwidth of 30 kHz).

Equation 15 gives the minimum gain bandwidth product of the correction amplifier. This is at least 45 MHz. According to (13) the dominant pole of the correction amplifier is at 1350 Hz.

As $H = \frac{1}{11}$, the first pole of the power block should be higher as 4 MHz.

3.1. The correction amplifier.

The demands on this amplifier are :

1. a high input impedance
2. a low output impedance
3. a stable gain
4. a higher slew rate than that of the whole amplifier
5. a higher output swing than that of the power block

A simplified conceptual circuit diagram is shown in fig. 12. The input stage is a differential pair T_1 and T_2. T_1 is loaded with a current mirror T_3 . . . T_8. The current in the cascode T_9 is α times the current in T_1. The gain of this amplifier is therefore only dependant on the D.C. current in the input stage and on the charge at the output of the cascode. This is the capacitor of 120 pF which gives in combination witht the output impedance of the cascode the dominant pole of the amplifier. The output stage is a klass-A mos power fet that provides for a very low output impedance and a very high input impedance.

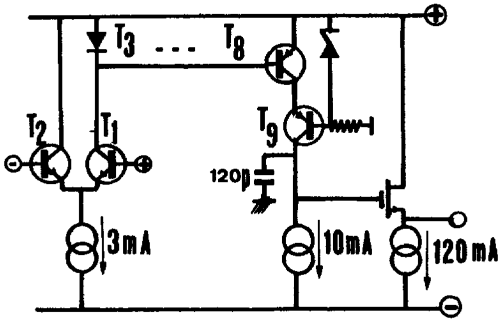


Fig. 12 : A simplified diagram of the correction amplifier.

A detailed circuit of this amplifier is given in fig. 13. The op-amp in this figure has nothing to do with the current dumping amplifier. Its task is to amplify the input signal 9 times.
Characteristics are as follows :

- Gain bandwidth product : 200 MHz.
- Slew rate : 80 V/μ s
- Output impedance : 5 ohm
- Maximum output current 120 mA.
- D.C. power dissipation : 32 W.

3.2. The power block

A circuit diagram is given in fig. 14. It has the next properties :

1. A high input impedance. This means that the charge on the correction amplifier is minimum. Distortion due to the fact that the output impedance of the correction amplifier is not zero will be insignificant.
2. There is no quiescent current in the output transistors. This gives a lot of cross-over distortion, but there are no thermal problems possible in this stage.
3. This block is built with very cheap bipolar transistors.
4. It uses a class-G configuration which has a higher efficiency than

the class-B stage. This is explained in ref. 3. As the output devices are very slow, a lot of switching distortion is seen at the output when the power block switches from the lower to the higher supply. This distortion can be reduced by the introduction of the coils in series with the lower supplies.

Fig. 16 shows the output signal of the power block. The input is a sine wave of frequency 20 kHz with low distortion. This picture shows also the difference between input and output. This waveform shows that there is a lot of cross-over and switching distortion.

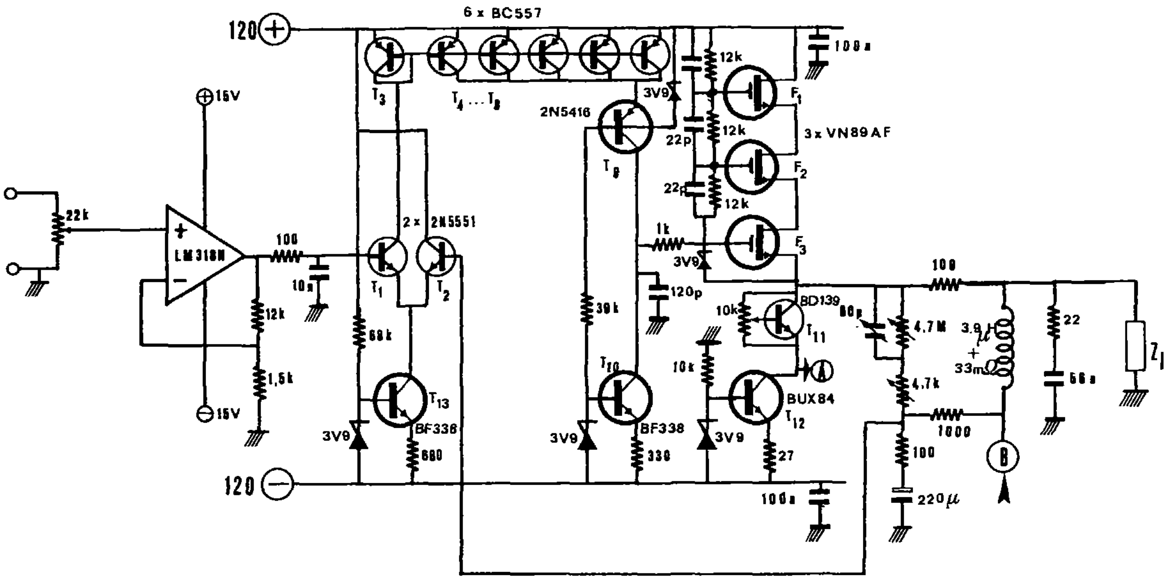


Fig. 13 : Sheme of the correction amplifier and the bridge components.

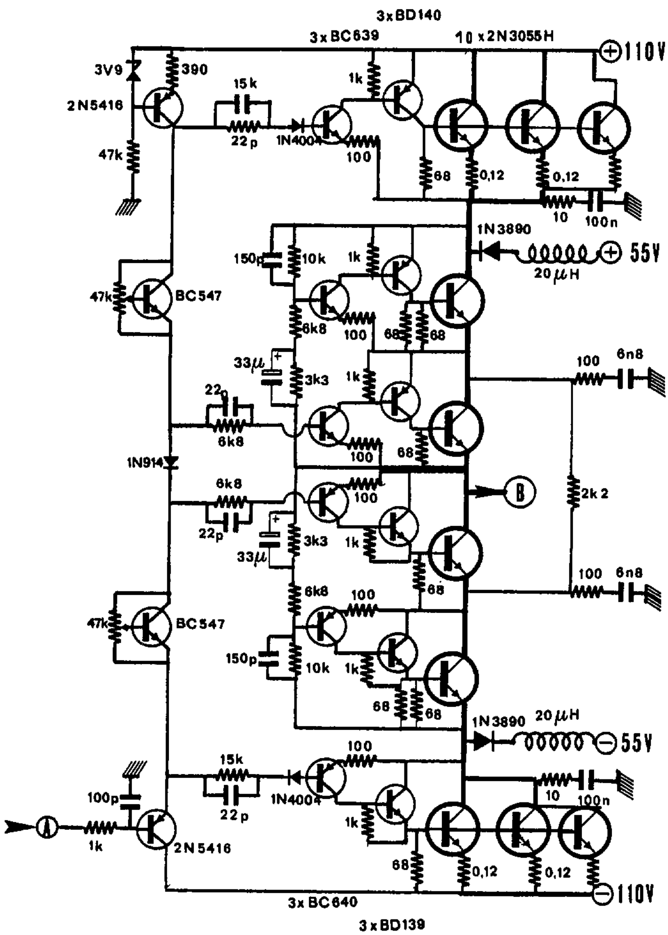


Fig. 14 : Sheme of the power block.

3.3. Experimental results.

Measurements are done with unstabilised supplies. At maximum output power there was a rippel of 15V at the + and - 110 V supplies.
The components of the impedance Z_2 were carefully adjusted for minimum distortion at the output signal.

With a load of 8 ohm this amplifier has the next properties :

Maximum output power	506 W
Small signal bandwidth	7 Hz ... 150 kHz
Power bandwidth	7 Hz ... 32 kHz
Slew rate	25 V/ μs
Amplification	99 X
Noise	-98 db (500 W)
Output impedance	(0.033 ohm + 3.9 μH)// 100 ohm
T.H.D.	fig. 15

Also note that fig. 15 indicates that the distortion at high frequencies is less for 500 W than for 112 W. This is because at high frequencies and high output currents the output transistors cannot switch sufficiently fast and all of the current is supplied by the higher power supplies, and therefore in the output signal of the power block there is less switching distortion at very high output power and high frequencies.

Conclusion

A 500 W current dumping audio amplifier has been proposed. It has been proven that the current dumping principle is advantageous to build high power amplifiers with very low distortion and high efficiency using slow and cheap output transistors. We have shown that if a very fast amplifier is requiered for other applications then for audio, the correction amplifier must be able to deliver a considerable output current.
Our conclusion is that current dumping should be used extensively in audio amplifiers because it can achieve more performance then feedback alone can.

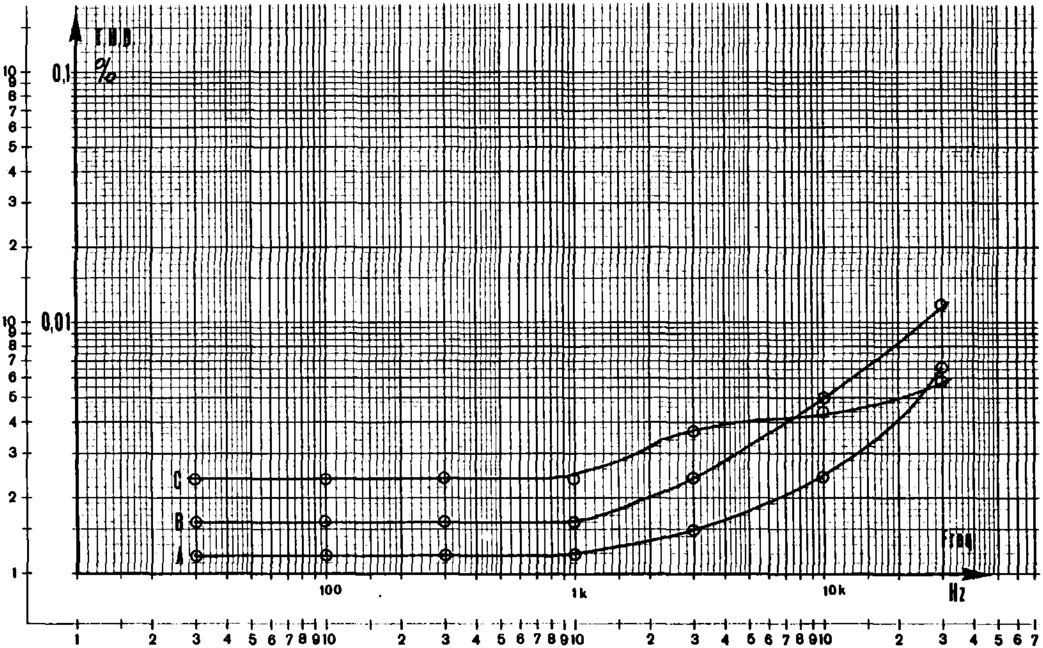


Fig. 15 : T.H.D. of the amplifier. Load is 8 ohm.

A : 100 W (80V ptp)

B : 225 W (120V ptp)

C : 506 W (180V ptp)

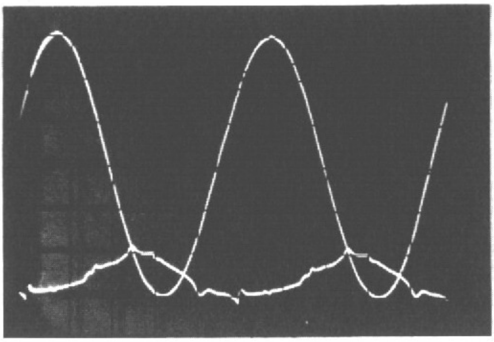


Fig. 16 : Output and distortion of the power block. Input is a sine wave of 20 kHz.
Output power is 500 W in 8 ohm. The lower trace is the difference between input and output. Scale is 5V/div. This trace shows the crossover and switching distortion.

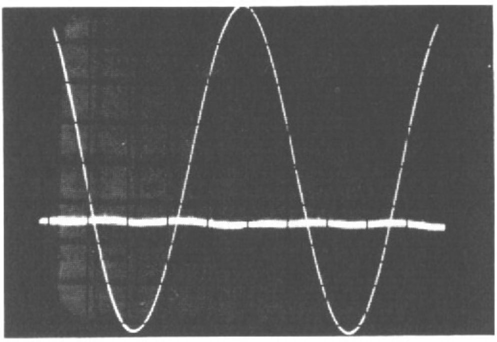


Fig. 17 : Harmonic distortion of the whole amplifier. Frequency is 1000 Hz. Output power is 500 W in 8 ohm.
T.H.D. = 0.0024%

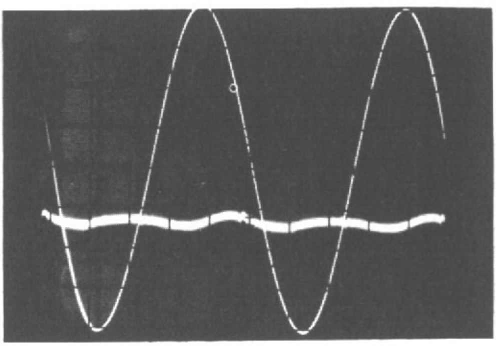


Fig. 18 : Harmonic distortion at 20 kHz. Output power is 500 W in 8 ohm.
T.H.D. = 0.005%

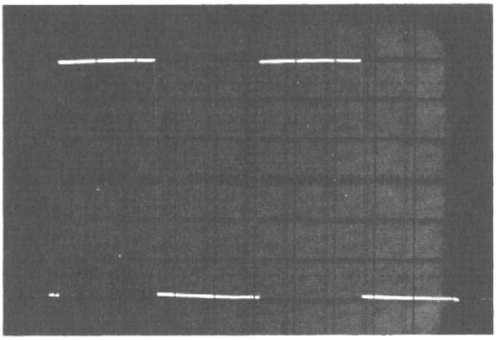


Fig. 19 : Square wave response
Frequency is 1000 HZ.

Scale : 20V/div.

Load is 8 ohm.

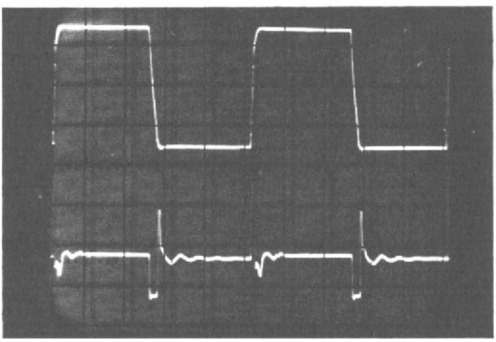


Fig. 20 : Square wave of 10 kHz.

Charge is 8 ohm.

Scale : 20V/div.

Lower trace gives the output current of the correction amplifier : 120 mA/div

This picture indicates the slew rate in current dumping amplifiers introduced by the inductor Z_4 and the limited output current of the correction amplifier.

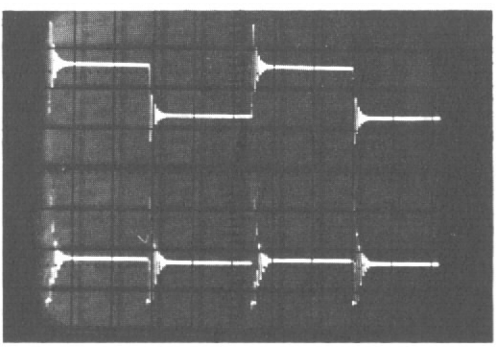


Fig. 21 : Square wave of 1000 Hz.

Charge is 16 ohm in parallel with 1 μF.

Scale : 20V/div.

Oscillations appear due to the inductive output impedance and the capacitive load.

Lower trace gives the correction current. 120 mA/div.

References

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