# POWER AMPLIFIER OUTPUT STAGE DESIGN INCORPORATING ERROR FEEDBACK CORRECTION WITH CURRENT DUMPING ENHANCEMENT

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## 0. INTRODUCTION

The design of high performance power amplifiers has devolved into two quasi-orthogonal schools. One school exploits the use of high levels of negative feedback which in general is applied in multiple loops following the work of Cherry[1] while the second philosophy attempts to minimise overall feedback and directs attention to the optimisation of each amplifier cell using distributive local feedback and corrective strategies[2,3].

Clearly, both philosophies offer merit and are each capable of good performance where no doubt purists will attempt to draw comparisons using canonical equivalents. In this paper we address some of the problems of the low feedback school as this offers an interesting challenge in the design of low distortion amplifiers especially in applications where transistors are exercised over a wide range of their dynamic characteristics. The momentum for this work has been spurred by the belief that amplifier performance should be near aperiodic and include only a minimum of extra energy storage devices to dictate the target transfer function.

A principle advantage of distributive feedback is that the active device characteristics can determine the stability of each stage without the addition of external compensation. It is also straightforward to configure low-level signal circuitry which exhibits excellent linearity together with well behaved non-linear overload with fast recovery. An earlier paper [2] reviewed some of the advantages of low feedback amplifiers and more recent work by Ottala [4,5] has discussed the interaction of distortion and the inevitable loop delay. It is probably worth reiterating that with pure negative feedback one is attempting to correct distortion retrospectively which is a dubious process at best. It is of concern that attempts to analyse combinations of amplifier nonlinearity and non-linear band limiting mechanisms with real signals prove extremely difficult. Consequently a design approach that circumvents some of the analytical problems may well lead to a more satisfactory conclusion.

In this paper we discuss further the application of error correction to the power amplifier output cell where it is shown that the technique can reduce both voltage transfer and current transfer distortion. Since

distortion correction requires the optimisation of a balance condition to minimise distortion then the sensitivity of adjustment is fundamental to the success of the technique. The paper will also discuss methods of de-sensitising the balance condition by the expedience of current dumping [6] and local feedback where effectively multiple zeros can be generated in the error function.

The work concludes by introducing circuit topologies that aid system realisation of the enhanced strategies as well as emphasising some of the finer design detail.

## 1. NON LINEAR DISTORTION IN THE FOLLOWER OUTPUT CELL

Bipolar junction transistors (BJT) are fundamentally transconductance devices exhibiting a high output resistance. It is only when they are configured in the classical follower configuration illustrated in Figure 1.1 that the output impedance is low as a result of near unity gain feedback.

The follower circuit will always exhibit a gain <1 when driving a finite load impedance (excluding near instability) thus there will be a finite error voltage $V_E$ between input and output. A further error signal will also result when the driving impedance is finite and this is compounded by signal dependency of the current gain.

It is possible to synthesise approximate distortion models though exact analysis is complex and a strategy for designing a reliable cascaded compensation network proves elusive. The problem results from the transconductance of the transistors being both emitter current dependent and temperature dependent. The thermal problem is of particular concern. It can be shown that the error voltage $V_E$ is both dependent upon the output current $I_o$ as well as the absolute temperature of each transistor, being particularly sensitive to the differential junction temperature. Consequently the error signal will in part include non-linear dependence on transistor thermal time constants, a problem which is aggravated when transistors dissipate high transient power under signal excitation.

In class AB amplifiers the magnitude of $V_E$ can be further increased when one or other output devices turns off though this can be reduced by non-switching configurations [8]. It is also worth noting that even under class A operation $V_E$ is finite though the error should tend to a linear function of the output current $I_o$.

The remainder of this paper addresses the problem of compensating for

the error signal $V_E$ where we commence by summarising the following observations:-

(a) Correction is applied locally to the output stage thus minimising further intermodulation of output cell distortion and signal in stages that share a component of output distortion through feedback.

(b) Correction is only applied when $V_E \neq 0$, it therefore follows the spirit of the low feedback school.

(c) The nature of $V_E$ including thermal dependence within bounds commensurate with error amplifier distortion, is unimportant.

(d) The technique can be used within an overall feedback amplifier to reduce transient phase modulation due to output stage non linearity.

(e) The technique, when optimised, decouples non-linear load impedances from the amplifier driving stage even if modest overall feedback is applied.

(f) The correction signals do not flow through the power supply thus aiding suppression of power supply induced distortion and simplifying the error signal path.

## 2. ERROR DISTORTION CORRECTION WITH FEEDBACK ENHANCEMENT

The basic topology of an error feedback correction loop has been the subject of previous reports [2,3]. One potential disadvantage of the technique is the degradation in performance that occurs through misalignment of the balance condition for minimum distortion, this can result from poor design, component aging or dynamic variation of the balance condition with signal i.e. secondary distortion within the error amplifier.

In this section we explore the sensitivity of the correction loop to alignment errors and show through the expedience of a second, local error feedback loop that the sensitivity can be reduced.

The system diagram of error feedback which is a subset of the more general feedforward-feedback structure [2] is shown in Figure 2.1 where N represents the voltage amplification of the output cell wher $N \cong 1$.

It has been shown [2] that the voltage amplification A (see Fig. 2.1) is given by

$$A = \frac{N}{(1-a) + aN} \qquad \ldots 2.1$$

where the balance condition is defined as a = 1: making A = 1.

It is constructive to decompose A into its optimum value and an error gain component $A_E$, where for a near unity gain amplifier,

$$A = 1 + A_E \qquad \ldots 2.2$$

Defining an error function E,

$$E = \frac{A_E}{A} = -(1-a)\left[\frac{1-N}{N}\right] \qquad \ldots 2.3$$

Differentiating E with respect to a and N, the sensitivity to misalignment and distortion can be explored, i.e.

$$\frac{\partial E}{\partial a} = \frac{1-N}{N} \qquad \ldots 2.4$$

$$\frac{\partial E}{\partial N} = \frac{1-a}{N^2} \qquad \ldots 2.5$$

We follow similar procedures in later analyses where equations 2.3, 2.4 and 2.5 form benchmarks.

Equation 2.4 and 2.5 both reveal significant sensitivity to error amplifier gain a. Consequently, moderate misalignment of a will incur a distortion penalty if $N \neq 1$, together with a secondary source of distortion if a undergoes dynamic modulation by the error signal. However, we note the favourable condition that the error amplifier loading factor[2] is minimised as $N \to 1$.

Consider next the modified structure shown in Figure 2.2 where a second error-difference loop is configured to augment the basic correction loop. We will show in Sections 3, 4 and 5 that the second loop can be implemented readily within the output stage circuitry. We also emphasise the intention that the level of feedback applied with the second loop is of modest level thus allowing wide near-aperiodic performance, with the ultimate performance bound being determined by inherent transistor characteristics.

In observing the structure of Figure 2.2, it is important to note the subtle distinctions between the error feedback loop and the secondary feedback loop. In the first loop, the correction is added prior to the distorting stage N, while in the second loop the error signal is added between the input and output nodes, it does not therefore introduce a further error function zero but simply desensitises the voltage gain from displacement in N and a.

Levels of secondary distortion are also reduced using the technique of Figure 2.2 as neither amplifier a nor amplifier b are exercised when N = 1, a condition that should be observed in the design of the output stage.

The voltage amplification $A_f$ of the enhanced topology can be shown to be,

$$A_f = \frac{N(1+b)}{\{(1-a) + N(a+b)\}} \qquad \ldots 2.6$$

where b is the differential gain of the secondary feedback loop. Following a similar decomposition of $A_f$ as illustrated by equations 2.2 and 2.3, we derive a modified error function $E_f$, where

$$E_f = - \frac{(1-a)(1-N)}{(1+b)(N)} \qquad \ldots 2.7$$

The sensitivities of $E_f$ with respect to a and N follow as,

$$\frac{\partial E_f}{\partial a} = \frac{(1-N)}{(1+b)N} \qquad \ldots 2.8$$

$$\frac{\partial E_f}{\partial N} = \frac{(1-a)}{(1+b)N^2} \qquad \ldots 2.9$$

Compared with the results of the basic correction system a reduction in sensitivity by a factor $(1+b)^{-1}$ is realised both for dynamic variation of N with signal and for secondary distortion due to modulation of a.

## 3. ERROR FEEDBACK DISTORTION CORRECTION WITH CURRENT DUMPING ENHANCEMENT

The previous section showed at the system level an enhancement over pure error feedback by introducing a secondary local error feedback loop. However, earlier papers [6,7] have cited a method of error feedforward correction colloquially designated "current dumping". This technique has been pioneered by Peter Walker and has generated much technical discussion [9]. A similar derivative was later implemented by Sansui [10].

Here we combine the technique of enhanced error feedback correction and current dumping to realise a further reduction in sensitivity to system misalignment. To clarify the operation of the circuit techniques discussed in Section 5 we introduce the enhanced system using a semi-circuit

presentation as illustrated in Figure 3.1.

The error feedback circuitry uses a transconductance amplifier ($g_m$) in association with $R_1$ while transistor $T_1$ operates as a unity gain follower with its collector current controlling the two-output port current mirror. The current mirror sources two currents: a feedback enhancement current mI, following Section 2 and a current dumping correction current nI.

We proceed by defining parameters p, q, r where initially transistor $T_1$ is assumed to have zero base emitter voltage, i.e.

$$p = \frac{nR_o}{(1+m)R_2} \qquad \ldots 3.1$$

$$q = g_m R_1 \qquad \ldots 3.2$$

$$r = \frac{mR_1}{(1+m)R_2} \qquad \ldots 3.3$$

Hence assuming an output load impedance $Z_L$, the voltage transfer ratio $A_d$ is given by,

$$A_d\left[1 + \frac{R_o}{Z_L}\right] = \left[\frac{1+r + p(1-q)\left(\frac{1-N}{N}\right)}{1+r + (1-q)\left(\frac{1-N}{N}\right)}\right] \qquad \ldots 3.4$$

Expression 3.4 reveals if either p or q (or both) = 1, then $A_d$ is independent of N and the output impedance is $R_o$. Also misalignment or non-linear error in p and q is desensitised by r if r > 0.

Again following the technique of Section 1 (equations 2.2, 2.3) we define an error function $E_{fd}$ for the system both with feedback and current dumping enhancement, i.e. if

$$E_{fd} = \frac{A_d\left[1+\frac{R_o}{Z_L}\right] - 1}{A_d\left[1 + \frac{R_o}{Z_L}\right]} \qquad \ldots 3.5$$

then,
$$E_{fd} = -\left[\frac{(1-p)(1-q)\left(\frac{1-N}{N}\right)}{(1+r) + p(1-q)\left(\frac{1-N}{N}\right)}\right] \qquad \ldots 3.6$$

Note that in specifying equation 3.5, the term $\left[1 + \frac{R_o}{Z_L}\right]$ was included in the expression to avoid the complication of output attenuation due to $R_o$, which is a linear effect dependent upon the load impedance $Z_L$.

The sensitivities of $E_{fd}$ with respect to p, q and N follow as,

$$\frac{\partial E_{fd}}{\partial p} = \frac{\left(\frac{1-q}{1+r}\right)\left(\frac{1-N}{N}\right)\left\{1 + \left(\frac{1-q}{1+r}\right)\left(\frac{1-N}{N}\right)\right\}}{\left\{1 + p\left(\frac{1-q}{1+r}\right)\left(\frac{1-N}{N}\right)\right\}^2} \quad \ldots 3.7$$

$$\frac{\partial E_{fd}}{\partial q} = \frac{\left(\frac{1-p}{1+r}\right)\left(\frac{1-N}{N}\right)}{\left\{1 + p\left(\frac{1-q}{1+r}\right)\left(\frac{1-N}{N}\right)\right\}^2} \quad \ldots 3.8$$

$$\frac{\partial E_{fd}}{\partial N} = \frac{\left(\frac{1-q}{N^2}\right)\left(\frac{1-p}{1+r}\right)}{\left\{1 + p\left(\frac{1-q}{1+r}\right)\left(\frac{1-N}{N}\right)\right\}^2} \quad \ldots 3.9$$

The error function $E_{fd}$ expressed by equation 3.6 shows the amplifier to exhibit three zeros in the domain of p, q and N which are mutually orthogonal as indicated by equation 3.1 and 3.2. The desensitisation due to (1+r) should also be observed. These results indicate the level of enhancement possible and allow a prediction of overall system non linearity to be made.

However, the analysis assumed the non-linear output stage N to exhibit an infinite input impedance. Since in practice this will not be the case, we explore in the next section methods of accommodating modulation of a finite input impedance within the overall system structure.

## 4. MINIMISATION OF CURRENT TRANSFER NON LINEARITY

Since the voltage transfer ratio of the output cell N will distort it follows that the current transfer ratio will also be non linear. In Figure 4.1, the non linear stage N is shown with non linear input resistance $R_N$.

Let us assume that the amplifier produces an undistorted output $V_x$ (after error correction for example), it follows that the input current $I_x$ is given by

$$I_x = \frac{V_x}{(NR_N)} \qquad \ldots 4.1$$

Consequently distortion in $I_x$ follows from both N and $R_N$. In the previous sections we assumed $R_N \rightarrow \infty$, in this section techniques are developed which enable finite, non-linear variations in $R_N$ to be accommodated.

The technique is based upon an idea first cited in an earlier paper [2], though only a basic discussion was given. In essence a small series resistor senses the input current to N, then part of this error signal is used within the compensation loop.

The simplified system topology is shown in Figure 4.2 where the voltage $V_E$ includes both a component of the error voltage across N as well as the error voltage across the input current sensing resistor $R_3$.

The configuration also includes current dumping enhancement though to allow orthogonality in the error function zeros, two current mirrors are used. Non orthogonality implies that the input error current $I_x$ would appear in the current dumping correction current $nI_1$, thus increasing the loading factor on this stage and leading to a more complex interactive balance condition.

The error signal $V_E$ is defined with reference to Figure 4.2 as,

$$V_E = I_x R_3 + kV_x\left(\frac{1-N}{N}\right) \qquad \ldots 4.2$$

where $$k = \frac{R_y}{(R_x+R_y)} < 1 \qquad \ldots 4.3$$

Assuming transistors $T_1$ and $T_2$ to have zero base emitter voltage and defining parameters w, x, y, z where

$$w = kg_m R_1 \qquad \ldots 4.4$$

$$x = \frac{R_1}{R_3}\left\{\frac{k}{(1+m)(1-k)}\right\} \qquad \ldots 4.5$$

$$y = n\frac{R_o}{R_4} \qquad \ldots 4.6$$

$$z = \frac{mR_1}{(1+m)R_2} \qquad \ldots 4.7$$

then analysing the circuit of Figure 4.2 where $V_x$ is the output of N, it follows that

$$B = \frac{V_x}{V} = \frac{(1 + z)}{(w+z) + \frac{1}{N}\left\{(1-w) + \frac{R_3}{R_N}\left\{(1-x) - \left(\frac{w-x}{k}\right)\right\}\right\}} \quad \ldots 4.8$$

If now we include the current dumping correction loop, then

$$\left(1 + \frac{R_o}{Z_L}\right)\frac{V_o}{V_{in}} = y + (1-y)\,B \quad \ldots 4.9$$

where once more following the form of equation 3.5 and defining the error function $E_{fo}$ for the present structure then

$$E_{fo} = \frac{-\left[(1-w)\left(\frac{1-N}{N}\right) + \frac{R_3}{(NR_N)}\left\{(1-x) - \left(\frac{w-x}{k}\right)\right\}\right](1-y)}{(1+z) + y\left[(1-w)\left(\frac{1-N}{N}\right) + \frac{R_3}{(NR_N)}\left\{(1-x) - \left(\frac{w-x}{k}\right)\right\}\right]} \quad \ldots 4.10$$

Expression 4.10 shows a strong resemblance to equation 3.6 but includes the non-linear input resistance $R_N$. In this configuration however, there are three balance conditions to be observed where for optimum performance $w = x = y = 1$ and $z > 0$.

We note that the expressions for the balance conditions yield orthogonality between w, y and N though w and x are linked. The latter effects only cancellation of $R_N$ and can be desensitised by the normal procedure of making $R_N >> R_3$. However, the total error is desensitised by making $z > 0$.

When the system of Figure 4.2 is close to optimum, equation 4.8 reveals $B \cong 1$ even though N exhibits both non-linear voltage transfer and non-linear current transfer, consequently the loading factor of transistor $T_1$ and the associated current mirror is minimised hence reducing secondary distortion. This result is important and is not inherent in conventional current dumping where the low power class A amplifier must always provide a proportion of the output current, at least with the Quad[6] configuration.

However, one problem area in configuring the second correction loop as pure current dumping is reflected in the choice of $R_4$ (Figure 4.2)

which can be evaluated using equation 4.6 with y = 1.

In practice $R_o$ is small ($\cong 0.1\Omega$) to minimise the output impedance of the amplifier, which implies a low value of $R_4$ or a high value of n. This latter requirement has ramifications in the choice of quiescent current of the feedforward correction amplifier both with respect to its magnitude and offset stability. However, feedforward correction is particularly applicable at high frequency where feedback error correction will fail due to bandwidth constraints.

We therefore propose to modify the structure of Figure 4.2 to include both feedback and feedforward error correction where the feedforward loop will become dominant at high frequency. The new topology is shown in Figure 4.3. In this sense the parallel with the Quad approach should be observed and the similarity is acknowledged [6]. However, note the distinction, the error signal is measured directly across the output stage, thus correction is only applied when there is a voltage difference between input and output stage. In the Quad configuration, the pre-output stage amplifier is included within the differencing amplifier, thus true error feedback is not implemented as the error signal is effectively added between the differencing nodes (i.e. input and output of the dumping transistors).

In Figure 4.3, transistor $T_1$ and resistor $R_4$ yield a current $I_1$ which is proportional to the total output stage error voltage $V_{ET}$. A fraction of this current $n_1 I_1$ is then fed back to the input stage where it is combined with the input signal current $g_1 V_1$.

Thus we proceed by establishing $V_o$ as a function of the new input $V_1$ but including the contribution from the secondary error feedback-feedforward loop shown in Figure 4.3.

Neglecting the small base current of $R_1$, then

$$\frac{V_o}{V_1} = \frac{g_1 Z_i}{\left[1+\frac{Z_o}{Z_i}\right]} \cdot \left[\frac{BR_4 + n_2 Z_o(1-B)}{R_4 - n_1 Z_i(1-B)}\right] \qquad \ldots 4.11$$

Defining an error function $E_{f1}$ and again following the form of equations 2.2, 2.3 then,

$$E_{f1} \cong \frac{-(1-B)\left[1 - \frac{(n_1 Z_i + n_2 Z_o)}{R_4}\right]}{\left[1 - \frac{n_1 Z_i}{R_4}(1-B)\right]} \qquad \ldots 4.12$$

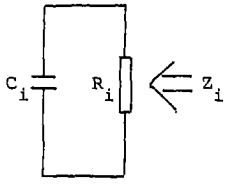
where B is the gain of the enhanced output stage and is defined by eqn. 4.8.

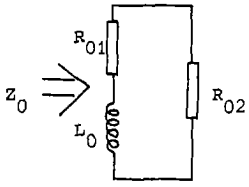
Equation 4.12 shows the balance condition of the secondary loop to be given by,

$$R_4 = (n_1 Z_i + n_2 Z_o) \qquad \ldots 4.13$$

Following Quad [6] we acknowledge that $Z_o$ can be made inductive which in turn can be compensated for by $Z_i$ being partly capacitive. Using these components a transition region between error feedback and error feedforward becomes possible which is advantageous for both correcting high frequency distortion and for maintaining a low output impedance.

As an example, suitable choices for $Z_i$ and $Z_o$ are illustrated below,




whereby given $n_1 n_2$, $R_i$ and $R_4$

$$R_{01} = \frac{R_4(R_4 - n_1 R_i)}{n_1 n_2 R_i} \qquad \ldots 4.14$$

$$R_{02} = \frac{R_4}{n_2} \qquad \ldots 4.15$$

$$L_o = \frac{C_i R_4^{\,2}}{n_1 n_2} \qquad \ldots 4.16$$

This section has illustrated how a unity gain follower output stage may be linearised by using an enhanced error correction topology. We can assess the effectiveness of this strategy by noting the cluster of zeros that appear in the error function $E_{f1}$, eqn. 4.12, where orthogonality is advantageous both from design optimisation and from the effects of secondary distortion due to non linearity in the correction amplifiers. In particular, with the secondary error feedback-feedforward structure of Figure 4.3, the low loading factor of the optimised B amplifier should be observed together with the ability to limit the bandwidth of the error feedback loop for good stability yet extend the high frequency correction using the wide band feedforward loop.

In the following sections we illustrate how these techniques could be implemented and suggest their possible application in high efficiency amplifier configurations.

## 5. CIRCUIT TOPOLOGY OF UNITY GAIN POWER OUTPUT CELL

Several derivatives of error correction topologies have been introduced in the previous sections. Here we attempt to translate these ideas into basic circuitry and to discuss further techniques for enhancing performance.

The target is to implement a system based upon Figure 4.2, together with the enhancement of Figure 4.3. We will proceed by discussing an implementation of Figure 4.2 that excludes for clarity the current dumping feedforward correction loop ($T_1$,$R_4$,$R_o$,n).

Transistors $T_2$ and $T_3$ form a Darlington buffer to reduce loading on the pre-output stage and to supply drive current via $R_1$ and $R_3$ to the Darlington output transistors $T_7$. Consequently transistors $T_2$ supply significant current to the bases of $T_7$ and are a source of distortion. To minimise $V_{BE}$-$I_e$ non linearity of $T_2$, the transistors are enclosed within a local feedforward correction loop formed by $T_3$ and $T_4$ where $T_3$ seconds as the first stage of the Darlington. However, we note that transistors $T_2$ and $T_3$ are enclosed within a local negative feedback loop using the(Xm)current mirrors, this further linearises $T_2$ and reduces the effective source impedance presented to the output transistors $T_7$. The resistor $R_1$ allows the error correction signal derived from the output cell to be superimposed on the input signal.

The main output transistors are shown operating at low collector base voltage which remains approximately constant due to the transistors $T_8$. This mode of driving decouples supply rail variation reduces power dissipation and minimises bias drift and thermally related distortions in the output transistors $T_7$. Since $T_7$ are operated at low collector base voltage, fast output transistors may be selected which can be placed in close physical proximity to the drive circuitry.

The output transistors are biased using transistors $T_6$ in an "amplified diode" configuration where the base emitter voltage of these two transistors forms the reference voltage. However, transistors $T_6$ together with $T_5$ also form the error amplifier for the output stage where their collector currents are circulated through resistors $R_1$ to add in the error correction signal. The advantage of this technique is that the error signal does not demand extra current from $T_2$, which was a feature of an earlier circuit [ 2 ]. Distortion in the driver stage is therefore reduced as well as keeping the signal paths both simple and local. It should be noted that the inclusion

of resistors $R_3$ allows current transfer non linearity to be compensated as discussed in Section 4. To enable the stability of the error correction feedback loop to be maintained, an impedance $Z_C$ (parallel combination of inductance/resistance) is introduced into the emitter circuit of the $T_5$, $T_6$ difference amplifier. The problem of stability within an error feedback loop is given consideration in the Appendix.

Finally, we observe a further local feedback loop from the output node to emitters of $T_2$ via resistors $R_2$, this represents the enhancement discussed in Section 2 and is illustrated in the simplified diagram of Figure 3.1. The resistors $R_2$ also form a small but welcome feedforward signal path directly across the output stage.

To complete the output cell using a similar structure to the system of Figure 4.3, we include the secondary distortion correction enhancement scheme illustrated in simplified form in Figure 5.2, this includes the circuitry of Figure 5.1 though detail has been omitted for clarity.

Inspection of Figure 5.2 and Figure 4.3 will reveal the similarity where the current gains of the mirrors follow as,

$$n_1 = \frac{R_{11}R_{14}}{R_{12}(R_{11}+R_{13}+R_{14})} \quad \ldots 5.1$$

$$n_2 = \frac{R_{14}(R_{11}+R_{13})}{R_{15}(R_{11}+R_{13}+R_{14})} \quad \ldots 5.2$$

It is possible to increase the efficiency of the output stage by using an array of multiple supply rails and a form of Class C cascodé as illustrated in Figure 5.1 (transistors $T_9$). This effectively reduces the maximum collector base voltage of each output transistor thus minimising both secondary breakdown and power dissipation. The technique was first reported in [11] and later employed by Carver in the "cube" amplifier. Since the cascode connection appears outside the correction loop, transient distortion, when devices commutate should be controlled.

## 6. CONCLUSIONS

This report has presented extensions of the techniques of error correction in analogue power amplifiers where it was shown that local feedback with a secondary orthogonal correction loop can significantly desensitise the amplifier to misalignment.

A method of reducing current transfer distortion was cited. This method effectively suppresses the non linear image of the loudspeaker impedance as seen through the output cell and therefore removes the loudspeaker from the global amplifier circuit. It is important to note that this suppression was readily implemented within the voltage transfer correction loop with minimal cost penalty.

The report further emphasised the link between error feedback and error feedforward where the deployment of the two procedures was frequency selective: feedback being dominant at low frequency with a gentle cross-over to feedforward at high frequency. With correct choice of linkage the error correction capabilities become aperiodic with minimal degradation due to bandlimitation of the feedback correction loop.

Analysis introduced the error function description of an error correction amplifier and showed directly the potential impairment due to malalignment of the balance condition. The positive advantages of multiple zeros in the error function could then be assessed together with the importance of orthogonality both from system design and system optimisation criteria.

Finally, introductory circuitry was presented which described methods of realisation. The circuits included enhanced distortion correction strategy together with further local correction to enhance linearity. Methods of improving efficiency and decoupling supply rail variations were also briefly discussed.

It is hoped the paper will further stimulate interest in the application of corrective procedures. The circuits are not intended as definitive only as vehicles for illustration and discussion. The author suggest these techniques form a realistic alternative to the high feedback school and significantly extend what can be achieved by simple local negative feedback.

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Appendix. Stability analysis of error feedback including equivalent topologies

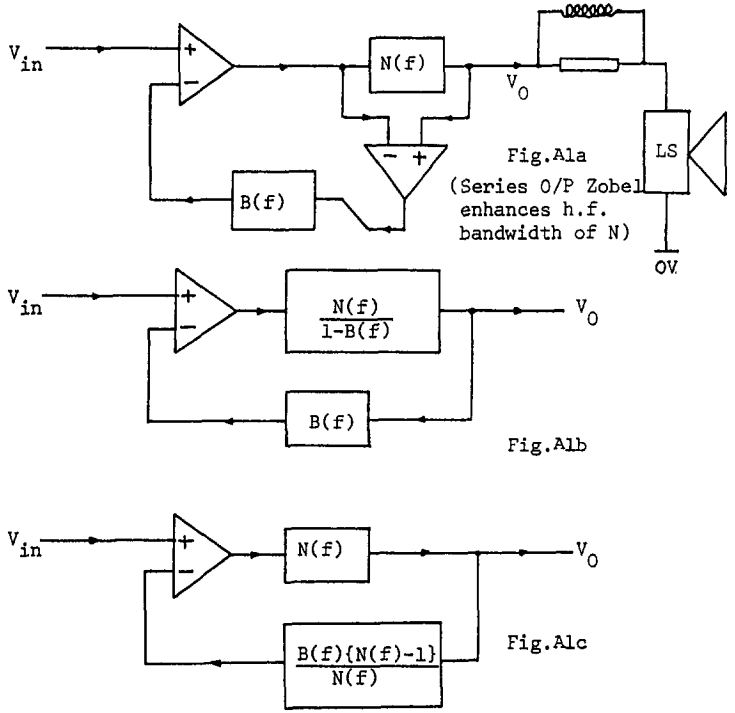



Figure A1 - Equivalent error feedback configurations

By analysis the closed loop gain G(f) and loop gains, $H_1(f)$, $H_2(f)$, follow, where:

$$G(f) = \frac{N(f)}{\{1-B(f)\}+B(f)N(f)} \quad \ldots\ldots A1$$

$$H_1(f) = \frac{N(f)B(f)}{B(f)-1} \quad \ldots\ldots A2$$

$$H_2(f) = B(f)[1-N(f)] \quad \ldots\ldots A3$$

It is interesting to compare the system in Figure A1b with Figure A1c. In the former we ideally require infinite gain in the forward path ($B(f) \approx 1$) whereas in the latter we have zero gain in the feedback path ($N(f) \approx 1$), yet both generate the same closed loop gain. On an initial consideration Figure A1b appears impractical whereas Figure A1c would appear eminently acceptable.

However, if we test for instability by equating the loop gain to unity then both equations A2 and A3 result in the condition:

$$B(f)[1-N(f)] = 1 \qquad \ldots\ldots \text{A4}$$

(for oscillation).

The output stage N(f) is, within the context of a power output stage, a near unity gain amplifier (e.g. a complementary emitter follower output stage with local negative feedback through emitter degeneration). However, the transfer function of N(f) will depend upon the load impedance (loudspeaker). For good control of the closed loop gain it is desirable to maximise the bandwidth of N(f). Basically this will be limited by the $f_T$ of the output transistors, however, by use of a series output Zobel network see Fig.A1a, (and/or feedforward across N(f)) the bandwidth can be extended such that to a good approximation,

$$N(f) = \frac{N_0(1 + j\frac{f}{f_3})}{(1 + j\frac{f}{f_1})(1 + j\frac{f}{f_2})} \qquad \ldots\ldots \text{A5}$$

The error amplifier can then be designed using wide bandwidth circuitry with local negative feedback and compensation (see circuit diagram in Fig.5.1) such that B(f) is a well defined first-order network where:

$$B(f) = \frac{B_0}{(1 + j\frac{f}{f_4})} \qquad \ldots\ldots \text{A6}$$

Generally $f_1 \approx f_T$ where $f_3$, $f_4 > f_1$. We also note that $B_0$ is close to unity, though in analysis account must be taken for values ranging, say, from 0.8 to 1.2 for stability and amplitude peaking under conditions of poor adjustment. From equations A4, A5 and A6 we deduce the following criteria for loop stability:

Let $f_n$ be the natural frequency of oscillation at unity loop gain;
$N_L$ the lower bound to $N_0$,
$N_u$ the upper bound to $N_0$.

1. For dc instability ($f_n = 0$)

$$N_L = (\frac{B_0-1}{B_0}) \qquad \ldots\ldots \text{A7}$$

2. For ac instability ($f_n > 0$)

$$f_n = \{f_1 f_2 (1+N_0 B_0 \frac{f_4}{f_3}) + f_4(f_1+f_2)(1-B_0)\}^{\frac{1}{2}} \qquad \ldots\ldots \text{A8}$$

$$N_u = \left[\frac{(\frac{f_1+f_2}{B_0 f_4})\left[1+\frac{f_4^2}{f_1 f_2}(1-B_0)(1-B_0)+(\frac{f_1+f_2}{f_4})\right]}{\left[1-\frac{1}{f_3}\{f_4(1-B_0)+(f_1+f_2)\}\right]}\right] \qquad \ldots\ldots \text{A9}$$

Conditions for stability:

Condition A $\quad N_u > N_L$

Condition B $\quad N_L < N_0 < N_u$

Condition C $\quad$ If $f_4 \to \infty$ then $f_3 < \left[\frac{N_0 B_0}{(B_0-1)(\frac{1}{f_1}+\frac{1}{f_2})}\right]$, $(B_0 > 1)$

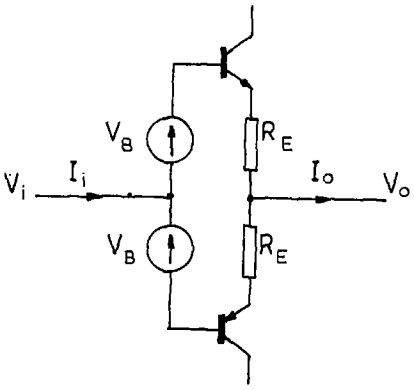
In practice, $N_0$ is just less than 1 (although it can be non-linear) and $(1-B_0) = 0$ to minimise distortion. For optimum performance it is important to maximise $f_3$ and yet keep high frequency peaking in the closed loop gain to within tolerable bounds. As an example, the following results are computed for a simulated example where:

$f_1 = 1\text{MHz}$, $f_2 = 20\text{MHz}$, $f_3 = 5\text{MHz}$

Table of Results ($P(N_0=x)$ => max. gain at $N_0 = x$).

| $f_4$ MHz | $B_0=1$ ($N_L=0$) | | | $B_0=1.2$ ($N_L=0.17$) | | |
|---|---|---|---|---|---|---|
| | $f_n(N_0=1)$ MHz | $P(N_0=0.8)$ dB (approx) | $P(N_0=1)$ dB (approx) | $f_n(N_0=1)$ MHz | $P(N_0=0.8)$ dB (approx) | $P(N_0=1)$ dB (approx) |
| 1 | 4.90 | 1.1 | 1.9 | 4.54 | 2.3 | 2.9 |
| 5 | 6.32 | 2.8 | 3.2 | 4.80 | 8.2 | 7.0 |
| 10 | 7.75 | 3.1 | 3.2 | 5.10 | 14.5 | 11.2 |
| 20 | 10.00 | 3.1 | 3.0 | 5.66 | 21 | 18.5 |
| 40 | 13.42 | 2.9 | 2.7 | 6.63 | 21 | 17.8 |

The results suggest that providing the bandwidth of N(f) is maximised then stability problems are minimal (practical circuit designs also corroborate this conclusion).




$V_i$ , input voltage
$V_o$ , output voltage
$I_i$ , input current
$I_o$ , output current
$V_B$ , bias voltage

Fig. 1-1 Follower configurations using complementory transistors

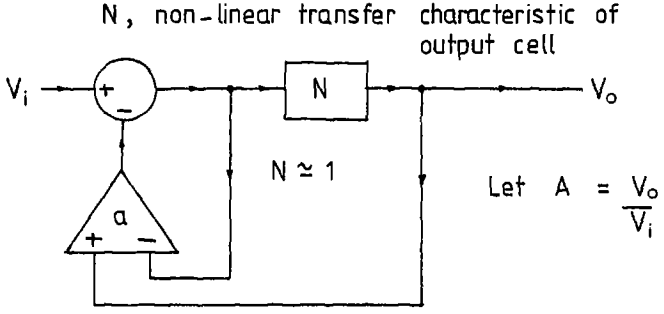



Fig. 2-1 Basic error feedback correction system

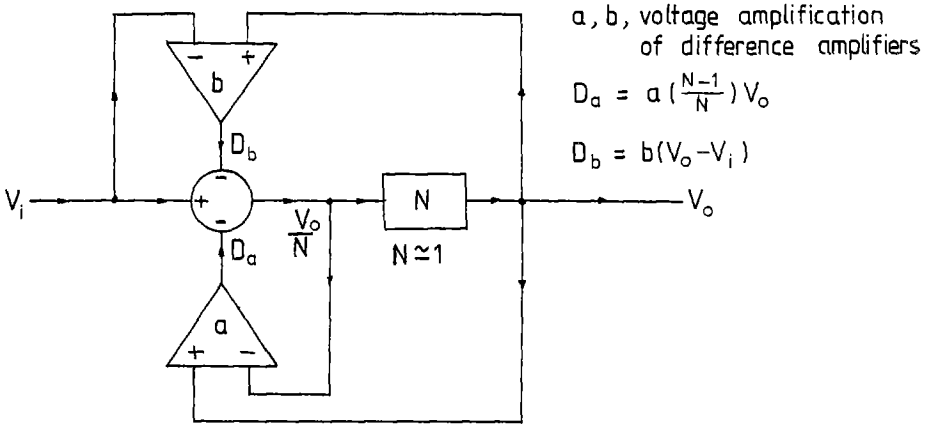



Fig. 2-2 Error correction feedback enhanced by secondary local feedback

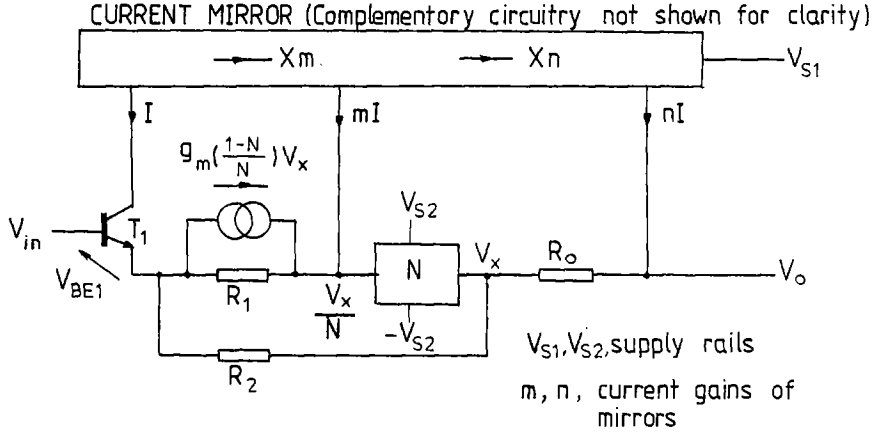
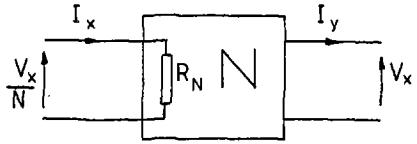



Fig. 3-1 Semi-circuit format of error feedback with current dumping enhancement




N , non-linear voltage transfer
$R_N$, non-linear input resistance
$I_x$, input current
$I_y$, output current
$V_x$, output voltage

Fig 4-1 Non-linear output cell

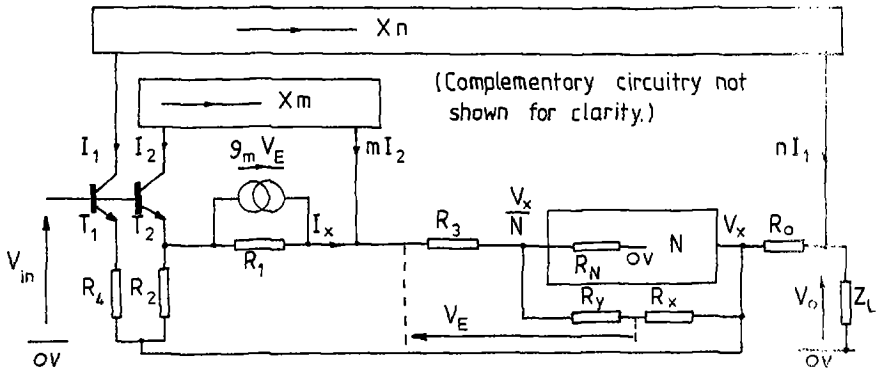



Fig. 4-2 Enhanced distortion correction with input error current compensation and current dumping

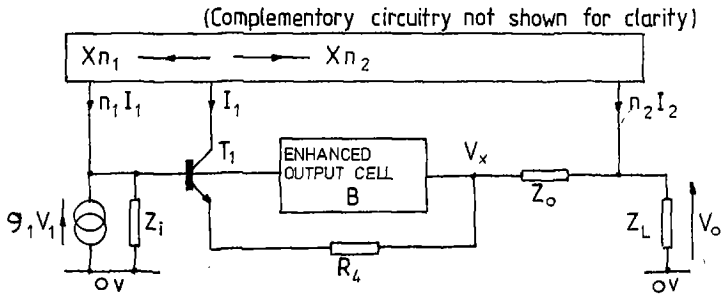



Fig. 4-3 Enhanced distortion correction using a secondary feedforward - feedback error correction loop

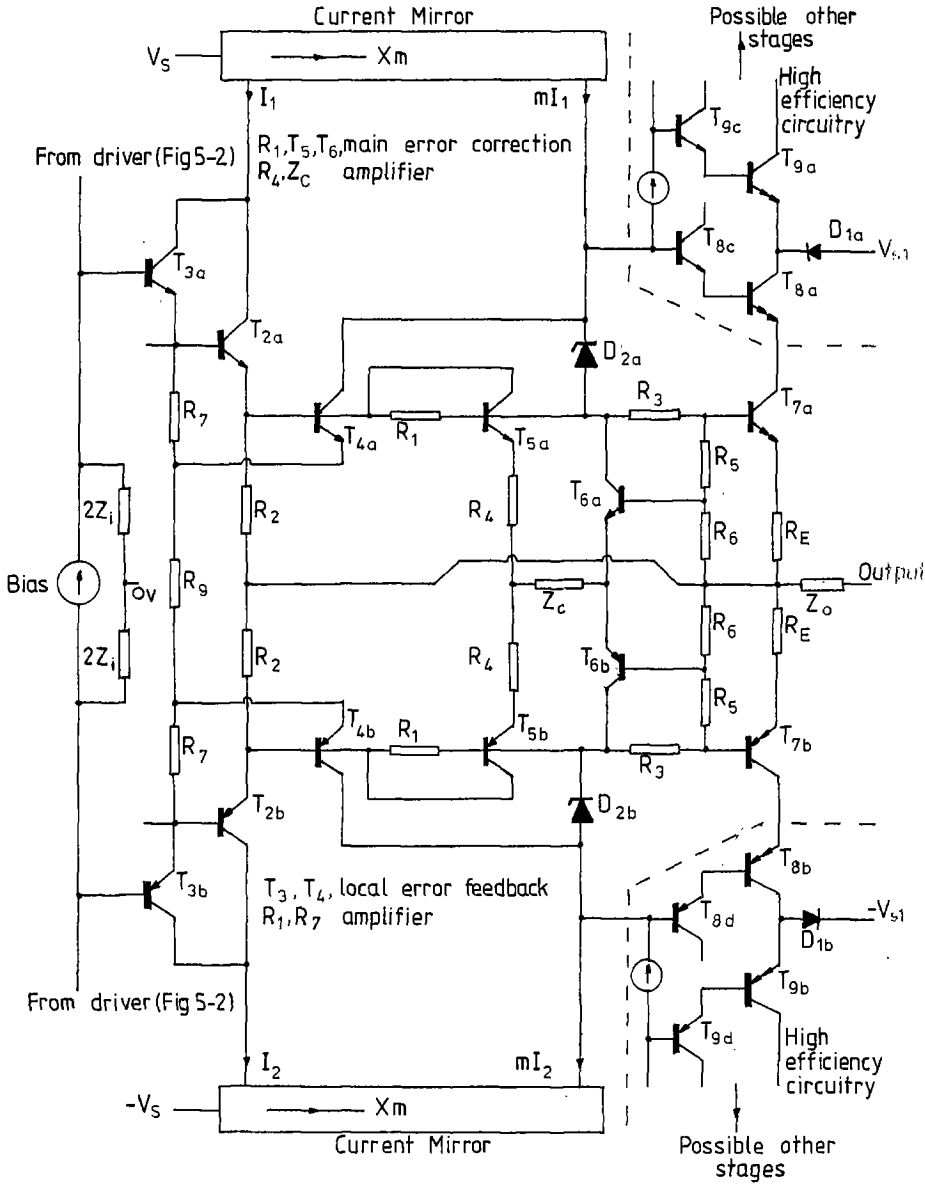



Fig. 5-1 Output cell with enhanced error feedback, input current compensation and high efficiency cascode circuitry

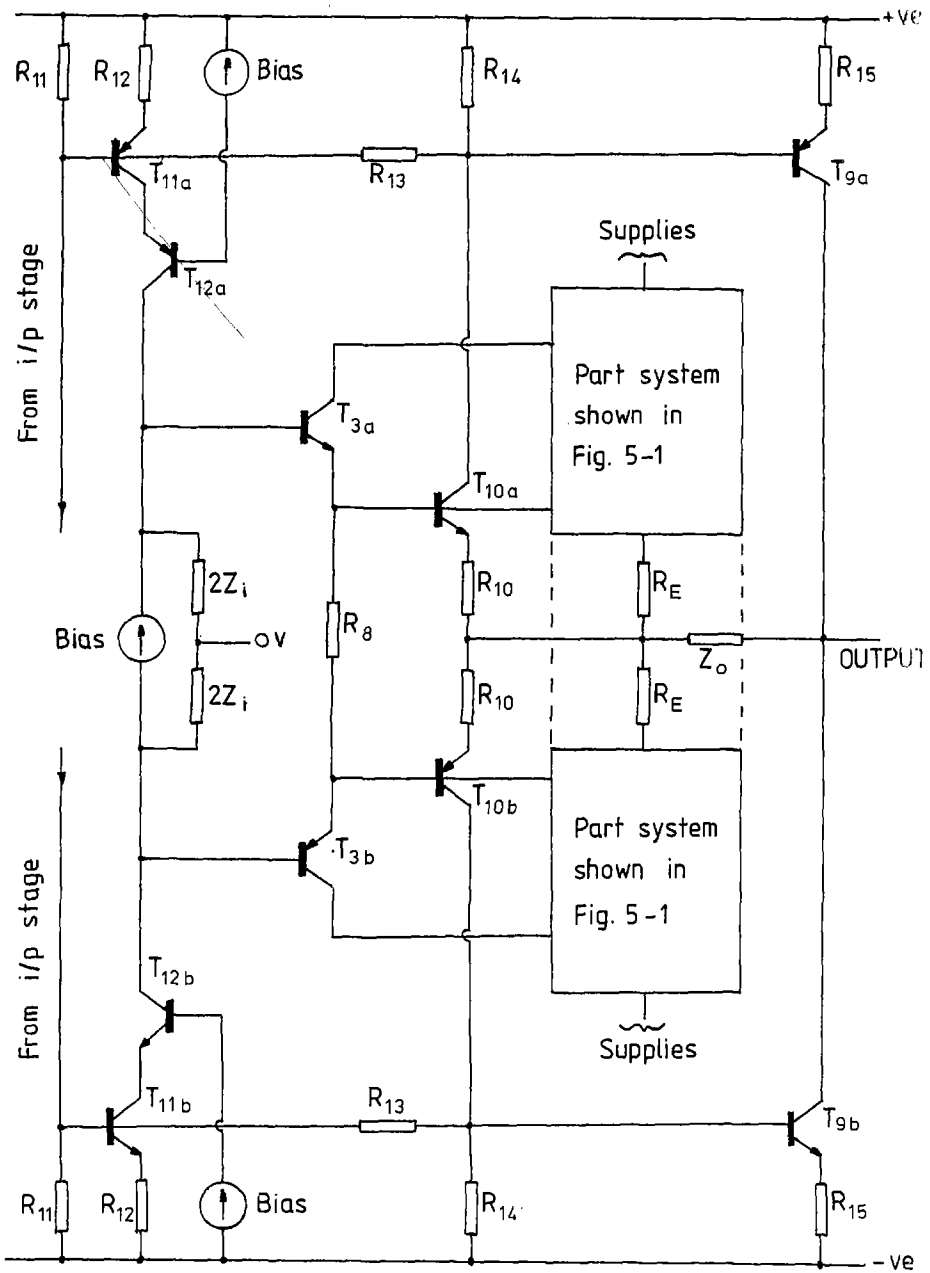



Fig. 5-2 System of Fig. 5-1 with further feedback - feedforward enhancement re Fig. 4-3