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A Current-Feedback Audio Power Amplifier

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ABSTRACT

A new low cost, high performance audio power amplifier topology that uses current-feedback in the main gain stage is described. This technique, which has previously been restricted mainly to wideband and video amplifier circuit design, improves on the more common voltage-feedback amplifier topology by providing a wide closed-loop bandwidth relatively independent of gain, and very high slew-rates. Measurements on the prototype power amplifier show that a closed-loop bandwidth of 1 MHz, at a gain of 24, and slew-rates in excess of 200 V/μs are readily achievable with inexpensive off-the-shelf components. In addition the in-band harmonic distortion is quite low (<0.002% at 1kHz), due to the large loop gain that is achievable at audio frequencies.

1. INTRODUCTION

Power amplification is a major requirement in almost every facet of the audio industry. From the high quality gear used for monitoring during mastering and mixdown, to the large and powerful sound reinforcement systems in use at live performances, not to mention the cost effective equipment designed for consumer reproduction, the need for power amplifiers is pervasive. Improvements in recording and reproduction technology during the past decade have placed increasingly heavier demands on amplifiers to deliver more power, provide greater dynamic headroom and above all to generate less distortion. Additionally, many new high quality loudspeaker systems have been introduced that can be particulary revealing when it comes to amplifier deficiencies.

As a consequence, numerous papers and articles over the years have reported on intensive engineering efforts directed at squeezing every last bit of performance out of existing linear power amplifier designs. Some of them have resulted in designs with truly impressive performance [1], albeit at the expense of greatly increased circuit complexity. Other radical designs have dispensed completely with the principles of global negative feedback and claim more "transparent sound", even though their distortion performance is usually inadequate. Most of the popular power amplifier designs, however, use the familiar voltage-feedback scheme made popular by the availability of modern IC op-amps. In fact, many audio power amplifiers are essentially discrete copies of monolithic op-amps like the 741 or 4136, but are usually simplified somewhat to cut down on the transistor count.

Almost all the technical improvements to these designs have *not* involved a complete re-thinking

of the overall amplifier design, but rather a selective patching up of the problem areas. Some designers have substituted novel input and gain stages for the more conventional ones [2], some have incorporated local error-correction circuits to linearize the output transistors [1], and still others have devised unusual output stage biasing schemes to lower crossover distortion [3]. But very little work, unfortunately, has been done to explore completely different *feedback* power amplifier topologies.

The purpose of this paper is to report on a new power amplifier design that does not use global voltage-feedback from the output back to the input stage. It also does not use only one feedback loop, but uses three. The dominant portion of the AC closed-loop gain is achieved through the use of a current-feedback loop, and the circuit borrows heavily from wideband amplifier design techniques. Voltage-feedback is used in the two other loops, but only for the low gain input-stage and the DC control amplifier. An economical design results from the use of IC op-amps in the input stage of the amplifier, while the rest of the circuit is composed of discrete bipolar devices driving a complementary MOSFET output stage. Also as a bonus, no expensive matched transistors are required. Although some audio purists might balk at the idea of a new amplifier design using multiple feedback loops and IC op-amps in the input stage, the measured performance of the prototype proves that the new topology is viable.

2. *CURRENT FEEDBACK VS. VOLTAGE FEEDBACK*

Monolithic and hybrid current-feedback amplifiers have become quite popular due to their desirable bandwidth versus gain characteristics. These characteristics need to be thoroughly examined before the new power amplifier circuit can be considered. To understand exactly how a current-feedback amplifier differs from a voltage-feedback amplifier, models of both types must be constructed and then analyzed to obtain the input-to-output transfer function. Once this is done, direct comparisons may be made between the two topologies.

A voltage-feedback operational amplifier can be modelled by the network shown in Figure 1. It contains a differential to single-ended converter, a transconductance amplifier, an RC compensation network and a unity gain output-buffer. The resistor R_o shown in the model is actually the effective parallel resistance seen at the output of the g_m stage due to all transistors connected to that particular node. The R_oC_c time constant sets the dominant pole of the amplifier and the product $g_mR_oA_{buf}$ is the open-loop DC voltage gain. Feedback is applied around the loop, from the output back to the inverting input, through the voltage divider formed by resistors R_1 and R_2. The expression for closed-loop voltage gain over frequency can be derived as follows:

$$V_o = \left(V_{in} - \left(\frac{R_1}{R_1 + R_2}\right)V_o\right)\left(\frac{g_m R_o A_{buf}}{1 + sR_oC_c}\right)$$

which may be written down by inspection of Figure 1. This leads to:

$$\frac{V_o}{V_{in}} = \frac{\left(\frac{g_m R_o A_{buf}}{1 + sR_o C_c}\right)}{1 + \left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{g_m R_o A_{buf}}{1 + sR_o C_c}\right)}$$

and finally, after some rearrangement:

$$\frac{V_o}{V_{in}} = \frac{1 + \frac{R_2}{R_1}}{\left(1 + \frac{(R_1 + R_2)/R_1}{g_m R_o A_{buf}}\right)\left(1 + s\left(\frac{R_o C_c}{1 + \frac{g_m R_o A_{buf}}{(R_1 + R_2)/R_1}}\right)\right)} \quad (1)$$

What this equation tells us is that the circuit has a DC closed-loop gain nearly equal to $1+ R_2/R_1$ (assuming that product $g_m R_o A_{buf}$ is reasonably large) and a closed-loop pole at a frequency of:

$$f_{pole} = \frac{1 + g_m R_o A_{buf}\left(\frac{R_1}{R_1 + R_2}\right)}{2\pi R_o C_c} \quad (2)$$

Thus one can see that the closed-loop pole frequency is actually equal to the dominant open-loop amplifier pole multiplied by one plus the loop-gain of the circuit. As the closed-loop gain is increased, the loop-gain drops in inverse proportion and so does the closed-loop pole frequency. The concept of a finite gain bandwidth product or unity-gain bandwidth that most manufacturers specify on their datasheets can therefore be expressed as a simple equation if R_1 is set to infinity (unity closed-loop gain):

$$GBW \cong \frac{g_m A_{buf}}{2\pi C_c} \quad (3)$$

This behavior is a fundamental characteristic of voltage-feedback amplifiers and presents some problems if one desires reasonably high gain and wide bandwidth at the same time. An additional

problem with voltage feedback amplifiers is that the slew-rate is usually restricted due to the fact that the transconductance stage has a finite maximum output current (usually equal to the tail current of the differential input transistor pair) available to charge the compensation capacitor. This can be a troublesome restriction in many audio power amplifier designs because it can lead to poor dynamic intermodulation distortion performance. High slew-rate is not only desirable but necessary as well, and necessitates large input stage tail currents and small compensation capacitor values. Unfortunately, in the interests of amplifier stability, reducing the value of the compensation capacitor necessitates degeneration of the input-stage to reduce the transconductance, which thus reduces the open-loop gain. This action reduces the amount of loop-gain available in the audio band and causes an increase in THD products, since it is the loop-gain that serves to reduce the open-loop amplifier distortion (most of which comes from the highly non-linear output-stage). An audio amplifier designer is thus faced with a dilemma, because a trade off between stability, open-loop gain and slew-rate must be made without compromising AC performance and transient response.

Current-feedback operational amplifiers were introduced primarily because they overcome the bandwidth variation, inversely proportional to closed-loop gain, exhibited by voltage-feedback amplifiers. Some variation of bandwidth is still observed, as the gain is increased from unity to moderate values, but is much less significant than with the latter. In fact current-feedback amplifiers don't begin to behave like voltage-feedback amplifiers, in this respect, until the closed-loop gain is made quite large. The concept of a finite gain-bandwidth product can also be applied to a current feedback amplifier as a measure of its performance, although it is only meaningful at high gains. Another feature of current-feedback amplifiers, is that the amount of current available to charge the compensation capacitor during output slewing is actually proportional to the difference between the actual and final output voltages (just like a simple RC circuit). As such, there is theoretically no slew-rate limit with this topology. Practical circuit limitations usually impose a restriction on the maximum current that can be handled in the input buffer and gain stages, however, and it is this limiting that gives rise to a finite slew-rate. Still, the slew-rates achievable with these types of amplifiers are almost always higher than those of their voltage-feedback counterparts for a given quiescent supply current.

To derive the input-to-output transfer function of a current-feedback amplifier, the representative model shown in Figure 2 must be analyzed. Instead of a differential input stage this topology utilizes a unity-gain input buffer, driving a low impedance current summing node, which forces the inverting terminal to be at the same potential as the non-inverting input. A non-zero input buffer output resistance, R_{inv}, is shown in series with the inverting terminal and must be included in the analysis of closed-loop gain versus frequency. Neglecting this resistance is a common mistake in simplified analyses, and leads to a transfer function that will not show any bandwidth variation with gain at all. Feedback is applied from the main amplifier output back to the inverting terminal through the current summing network consisting of R_1 and R_2. The action of the input buffer is to force a finite current through R_1 that must be balanced by an almost exactly equal but opposite current in R_2. Any difference between these two currents is an error current that flows into or out of the low impedance inverting terminal. This is then mirrored and fed into a transimpedance stage consisting of R_t and C_c, where current to voltage conversion takes place. The voltage generated here is buffered by another unity-gain stage and fed to the main amplifier output. Because the

value of the small-signal transresistance, R_t, is very high (normally several megohms), only minute error currents are needed to change the voltage at node 2 by several volts. Consequently, the amount of current that must flow into or out of the inverting terminal under steady state conditions is extremely small. The feedback network, even though it is made up of fairly low value resistors, therefore presents a very light effective load on the output of the input buffer. To derive a transfer function for this amplifier, KCL must be used at nodes 1 and 2. At node 1 we have:

$$\frac{V_1 - 0}{R_1} + \frac{V_1 - V_o}{R_2} + \frac{V_1 - V_{in}}{R_{inv}} = 0$$

which leads to:

$$V_1 = \frac{\frac{R_2}{R_{inv}} V_{in} + V_o}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{inv}}}$$

Doing a similar analysis at node 2 yields:

$$V_2 = \frac{I_1 R_t}{1 + sR_tC_c}$$

Now, some expression is needed to relate the output voltage to the voltages at nodes 1 and 2. This is a simple task, since:

$$I_1 = \frac{V_{in} - V_1}{R_{inv}} = V_1\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_o}{R_2} \qquad and \qquad V_o = A_{buf}V_2$$

Thus after the appropriate substitutions are done to eliminate V_1 and V_2, so that a relation solely in V_o and V_{in} can be obtained, we have:

$$V_o = \left(\left(\frac{\frac{R_2}{R_{inv}} V_{in} + V_o}{1 + \frac{R_2}{R_1} + \frac{R_2}{R_{inv}}}\right)\left(\frac{1}{R_1} + \frac{1}{R_2}\right) - \frac{V_o}{R_2}\right)\left(\frac{R_t A_{buf}}{1 + sR_tC_c}\right)$$

Unfortunately, the last equation tells us very little about the frequency response of a current-feedback amplifier since it is an implicit expression containing the output voltage term V_o. After some elaborate rearranging, however, a much more useful expression is obtained:

$$\frac{V_o}{V_{in}} = \frac{1+\frac{R_2}{R_1}}{1+\frac{R_2+\left(1+\frac{R_2}{R_1}\right)R_{inv}}{R_t A_{buf}}+s\frac{\left(R_2+\left(1+\frac{R_2}{R_1}\right)R_{inv}\right)C_c}{A_{buf}}} \tag{4}$$

Now this equation is in a form that is useable, but to make it look exactly like the closed-loop gain expression for a voltage-feedback amplifier, some simple rearrangment of the denominator is required:

$$\frac{V_o}{V_{in}} = \frac{1+\frac{R_2}{R_1}}{\left(1+\frac{R_2+\left(1+\frac{R_2}{R_1}\right)R_{inv}}{R_t A_{buf}}\right)\left(1+s\left(\frac{\left(R_2+\left(1+\frac{R_2}{R_1}\right)R_{inv}\right)C_c}{A_{buf}+\frac{R_2+\left(1+\frac{R_2}{R_1}\right)R_{inv}}{R_t}}\right)\right)} \tag{5}$$

This final result is now in the form of equation (1) and it can be seen that, as with a voltage-feedback amplifier, the DC closed-loop gain is also nearly equal to $1+R_2/R_1$ (assuming that the product $R_t A_{buf}$ is reasonably large). At a first glance the frequency dependent term would seem to be a large messy expression that gives little insight into the behavior of the amplifier. But since the small-signal transresistance (R_t) is so large, the closed-loop pole frequency can be written down in an abbreviated form without incurring a large error in the calculation:

$$f_{pole} \cong \frac{A_{buf}}{2\pi\left(R_2+\left(1+\frac{R_2}{R_1}\right)R_{inv}\right)C_c} \tag{6}$$

This result is very interesting because it shows that the pole frequency now depends predominantly on the value of the feedback resistor R_2, and the input buffer output resistance, R_{inv}, multiplied by the closed-loop gain. Normally the value of R_{inv} is made as low as possible to minimize the change in pole frequency with gain, and it is typically less than one tenth that of the recommended minimum feedback resistor value. At high gains, however, the closed-loop bandwidth starts to become inversely proportional to the gain because the term in the denominator of equation (6) due to R_{inv} becomes dominant. The gain bandwidth product is thus:

$$GBW = \frac{A_{buf}}{2\pi R_{inv} C_c} \tag{7}$$

The gain of the output buffer, A_{buf}, also plays its part in determining the closed-loop pole frequency. As the main amplifier output is loaded, this gain drops well below unity, and causes a reduction in closed-loop bandwidth as dictated by equation (6). This tends to make the amplifier more stable since the high frequency non-dominant poles contribute less phase shift at the lower closed-loop bandwidth. In fact many commercial current-feedback amplifiers show significant gain peaking with light loads, and don't begin to behave acceptably until loaded fairly heavily. Another thing to remember is that the minimum recommended value for the feedback resistor, R_2, must be strictly adhered to because too low a value will result in an excessively high closed-loop pole frequency. This can result in significant gain peaking due to the higher order poles in the amplifier becoming more dominant, and is especially a problem at low gains when the multiplicative effect of R_{inv} on the closed-loop pole time constant is minimal. Most manufacturers will normally state the suggested minimum value for R_2 on their datasheets.

The first commercially available current-feedback amplifiers, introduced in the early 1980's [4], [5], were very wideband hybrid devices intended for pulse and RF applications, and carried a high price tag. Later monolithic implementations [6] were lower bandwidth designs aimed primarily at the video amplification and high speed data-acquisition markets, and were priced much more reasonably. Use of these devices in audio equipment as gain stages and buffers has been almost non-existent, however. This is mainly due to the fact that their high slew-rate and wide bandwidth is really unnecessary in many cases, plus there are several good conventional audio op-amps already available at substantially lower cost. Power amplifier designs, on the other hand, can greatly benefit from the use of a current feedback gain stage.

3. POWER AMPLIFIER TOPOLOGY

Before delving deeply into the detailed operation of the power amplifier circuit a simplified block diagram, shown in Figure 3, will be considered to help understand how the overall design is partitioned. This will make the final amplifier circuit diagram easier to follow. As is evident from Figure 3, there are several fairly well defined functional blocks in this amplifer that can be discussed individually. These are:

A) The input stage: the input buffer used in this power amplifier is actually a conventional voltage-feedback op-amp chosen for its excellent audio characteristics, and its moderately high output current capability. This ensures that the limiting factor in terms of overall amplifier performance will be the current-feedback gain block and not the input stage. The output current from the input amplifier, A_1, is taken from its power supply pins and fed to the emitters of a pair of voltage regulator transistors (Q_1 and Q_2) connected in the common-base configuration. They, in turn, feed two current mirrors referenced to each supply rail. At an initial glance this might seem to be a very strange connection because the power supply pins of A_1 are used as outputs, and its output is used as an input. However, this is in accordance with the model shown in Figure 2 since the output current from the input buffer must be fed into the transimpedance stage which generates the output voltage prior to buffering. The half-wave rectification action of A_1's output current due to its class AB output stage causes the two current mirrors to receive complementary input currents. When A_1 is sourcing output current, it causes a corresponding increase in the current of the upper mirror and a decrease in that of the lower mirror. This causes the voltage at the output of the transimpedance stage to swing positive. For cases where A_1 is sinking ouput current, exactly the opposite is true. The common-base connected regulator transistors keep the supply voltage of the op-amp within its maximum operating limits and attenuate any fluctuations in the main supply voltage. The quiescent current of A_1 conveniently serves to bias the two current mirrors that sit referenced to each power supply rail, thus providing an appropriate DC operating point for the transimpedance stage and the bias voltage generator. Quiescent current of the op-amp used for A_1 in this power amplifier was about 5 mA.

In most hybrid and monolithic current feedback amplifiers the input buffer stage has a gain of unity and is generally an open-loop design. In this design an op-amp is being used as the input stage instead, and thus can be configured to provide some gain. This is extremely easy to do since it only involves tapping the shunt resistor, R_1, at the output of A_1. The overall amplifier mid-band AC gain is therefore:

$$A_v = \left(1 + \frac{R_{1A}}{R_{1B}}\right)\left(1 + \frac{R_2}{R_{1A} + R_{1B}}\right) \qquad (8)$$

B) The gain stage and compensation: the outputs of the two current mirrors that are connected to each supply rail feed an adjustable voltage bias-generator which provides the necessary bias for class AB operation of the MOSFET output stage. This bias-generator is designed to have very low output impedance over the operating frequency range of the amplifier. Compensation is provided by C_{c1} and C_{c2}, and two capacitors are used instead of one to keep the structure of the gain stage symmetrical. Unlike the current-feedback amplifier model shown in Figure 2, this design has the compensation capacitors returned to the feedback summing node as opposed to ground. This alternate connection has a very beneficial effect on the amplifier step response when it is loaded by a fairly low value impedance, such as a loudspeaker. A MOSFET source-follower output stage, such as the one used in this amplifier, has a transfer function that contains two poles and a zero plus the usual DC gain term [7]. When the amplifier drives high values of load impedance (ie just the feedback resistors) the two output stage poles are fairly high in frequency (above 30MHz), and contribute little excess phase shift at frequencies within the power amplifier's passband. This

causes the output to be very well behaved when a squarewave is applied to the input of the amplifier, because it acts mainly as a single-pole system. When the two compensation capacitors are connected to ground, the unloaded squarewave response of the amplifier is shown in Figure 4a and exhibits no overshoot or undershoot. The unloaded squarewave response of the amplifier with the compensation capacitors connected to the feedback summing node is shown in Figure 4b, and also reveals no traces of ringing. Connecting the two compensation capacitors either to ground or the feedback summing node thus appears to have very little effect on the shape of the overall response with no load. In fact it is difficult to differentiate between figures 4a and 4b.

A very different situation arises when a load (such as an 8 ohm resistor) is connected to the output. The two poles in the MOSFET output stage now split apart and the dominant one becomes sufficiently low in frequency that it contributes excess phase shift within the amplifier's passband. Now the amplifier starts to behave like a two-pole system and this causes the feedback loop to have reduced phase margin, plus all the attendant problems that are associated with it. When ground referenced compensation capacitors are used, the loaded squarewave response, shown in Figure 5a, exhibits an abnormal instability on the falling edge of the waveform. This behavior is undesirable in a power amplifier and eliminated the ground referenced compensation scheme from being considered for the final design. When the compensation capacitors are connected to the feedback summing node, however, the loaded amplifier squarewave response shows no sign of instability as Figure 5b indicates. This connection for C_{c1} and C_{c2} is thus the one of choice, and also allows the use of smaller capacitors than before. Analysis of the current-feedback model shown in Figure 2, but with the compensation capacitor connected to the feedback summing node, yields a new closed-loop transfer function very similar to equation (4):

$$\frac{V_o}{V_{in}} = \frac{\left(1+\frac{R_2}{R_1}\right)\left(1+s\left(\frac{2R_1R_2C_c}{R_1+R_2}\right)\right)}{1+\frac{R_2+\left(1+\frac{R_2}{R_1}\right)R_{inv}}{R_tA_{buf}}+s\left(\frac{2R_2C_c+\left(1+\frac{R_2}{R_1}+\frac{R_2}{R_t}\right)R_{inv}C_c}{A_{buf}}-R_{inv}C_c\right)} \quad (9)$$

The major difference between equations (4) and (9) is the appearance of a zero at a frequency determined by the parallel combination of R_1 and R_2, and the compensation capacitor C_c. Another interesting thing to notice is that the R_2C_c time constant, in both the numerator and denominator, is now multiplied by a factor of two instead of unity as before. Since it is this time constant that predominantly determines the closed-loop pole frequency, the capacitor values for C_{c1} and C_{c2} in Figure 3 may thus be scaled by a factor of one-half. To see how the new closed-loop transfer function is affected by the output stage response when loaded, A_{buf} may be replaced by a single pole

response:

$$A_{buf}(s) = \frac{A_{buf(DC)}}{1 + s\tau_{buf}}$$

Equation (9) may now be simplified and rewritten to reflect the output stage response:

$$\frac{V_o}{V_{in}} \cong \frac{\left(1 + \frac{R_2}{R_1}\right)\left(1 + s\left(\frac{2R_1R_2C_c}{R_1 + R_2}\right)\right)}{1 + s\left(\frac{2R_2C_c + \left(1 + \frac{R_2}{R_1}\right)R_{inv}C_c}{A_{buf(DC)}} - R_{inv}C_c\right) + s^2\left(\frac{\left(2R_2C_c + \left(1 + \frac{R_2}{R_1}\right)R_{inv}C_c\right)\tau_{buf}}{A_{buf(DC)}}\right)}$$

It can be seen that the new transfer function has two poles because the denominator is second order, but the the apperarance of the zero makes the overall transfer function revert to a first order response. The zero in the numerator would normally cause noticeable closed-loop gain peaking if the output-stage had excellent high frequency response, but in this case it does not, because pole-zero cancellation occurs at high frequencies. This compensation approach greatly helps to reduce the excess phase shift caused by the output stage, and results in an acceptable squarewave response unloaded or loaded. The frequency at which the zero occurs is approximately equal to the closed-loop bandwidth multiplied by the gain of the current-feedback loop, if R_{inv} is fairly small in value. Since the denominator of the above equation cannot be easily hand factored, the poles may be found by using a quadratic root-finding program.

C) Driver and output stages: This part of the power amplifier design is quite conventional, and no attempt was made to use error-correction or pseudo class A biasing schemes to lower the output stage crossover distortion. Since the primary design goal for this amplifier was wide bandwidth, it was felt that any unnecessary additional circuitry following the transimpedance gain stage might degrade the closed loop stability. A simple double emitter-follower stage therefore was chosen to buffer the voltage generated by the gain stage and feed it to the gates of the power MOSFETs. This driver stage is capable of providing several hundred milliamps of charging current for the MOSFET gate capacitances while the output is slewing, and is mandatory in a high-speed design. Although the MOSFET output stage could have been connected directly to the gain stage, as is the case with many simpler amplifiers, this would have caused the slew-rate to be limited to somewhat less than 30 V/µs because the effective gate capacitance of the output devices is quite large. The gate-to-drain capacitance plus the bootstrapped gate-to-source capacitance for just the single pair of MOSFETs used in the prototype amplifier is over 1000 pF. If multiple pairs of output devices are used, as would be the case in a very high power amplifier, the slew-rate would be degraded even further without the driver stage.

D) DC control amplifier: The purpose of this stage is to provide an accurate, low-drift, DC gain path to the main output that is independent of the AC gain path and its inherent DC instability. In the original version of this amplifier precision matched NPN and PNP transistors were used in the two current mirrors, but no DC control amplifer was used. It was assumed (incorrectly) that precision matching of the transistors in each mirror would result in a very low output-offset voltage, as long as the input buffer had reasonably low input-offset voltage. Unfortunately, this is not the case with a current feedback amplifier. Any mismatch between the two current mirrors results in a finite amount of bias current appearing at the output terminal of the input buffer, which must flow through the feedback resistor, R_2, to the output. It cannot flow through R_1 because the current in this resistor is set only by the voltage appearing at the output of the input buffer. The output offset voltage, without the DC control amplifier, is thus:

$$V_{oos} = V_{ios(A1)}\left(1+\frac{R_{1A}}{R_{1B}}\right)\left(1+\frac{R_2}{R_{1A}+R_{1B}}\right)+I_{bias}R_2 \qquad (10)$$

Normally $V_{ios(A1)}$ can be made quite small by using a low-offset op-amp. Unfortunately I_{bias}, the inverting terminal bias current, can be as large as 100 μA under static conditions and even larger if a thermal gradient exists between the the two current mirrors on the power amplifier circuit board. This can easily lead to an output offset in excess of 100 mV, that changes as the amplifier warms up. A large offset like this is very undesirable since it will result in an audible click when the relay that connects the loudspeaker to the amplifier output is energized.

The solution to these problems is made possible by the use of a low-power precision op-amp, A_2, configured as an integrator with a very low crossover frequency (less than 5 Hz). This low crossover frequency ensures that the integrator will not have any effect on the performance of the overall amplifier in the audio band. Voltage-feedback is applied from the main output back to the input of the integrator, through resistors R_3 and R_4, and thus they set the closed loop DC gain. This gain is made equal to that given by equation (8). Since the A_2 drives a resistor connected to ground, as shown in Figure 3, it behaves as an operational transconductance amplifier with the output current taken from its power supply terminals. This compensating current is then fed into the two common-base regulator transistors where it is summed with the signal current from the power supply terminals of A_1. The output current of A_2 therefore is forced to cancel I_{bias} almost exactly because the DC gain of the integrator, coupled with the additional gain produced by the transimpedance stage, is very high. Consequently, the integrating control-loop overrides the current-feedback loop at DC and the output offset voltage is reduced from that given by equation (10) to:

$$V_{oos} = V_{ios(A2)}\left(1+\frac{R_3}{R_4}\right) \qquad (11)$$

which means that it can be made arbitrarily small by the use of a low offset amplifier for A_2.

4. POWER AMPLIFIER CIRCUIT DESIGN

The complete circuit diagram of the current-feedback power amplifier is shown in Figure 6. It uses two IC op-amps, seventeen bipolar transistors in the gain and driver stages, and at least two power MOSFETs in the output stage. The driver stage can easily accommodate multiple pairs of power devices in the output stage, because of its high current drive capability, but just a single pair of MOSFETs was used in this version. Most of the components that mount on the compact driver board, shown in Figure 7, are readily obtainable and quite inexpensive.

An input filter with a cut-off frequency of approximately 2MHz was used on the prototype amplifier to eliminate potentially troublesome RF interference, and also to prevent the possibility of the amplifier oscillating on power-up when the input was left floating. This filter is formed by the 100Ω input resistor and the 750pF shunt capacitor. A 100kΩ resistor is connected to ground at the input of A_1 and provides the necessary DC bias current path to ground if the input is inadvertently left open. The overall gain is set by R_6, R_7 and R_8, and substituting the values of these resistors into equation (8) yields a figure of 24.087 or 27.64dB. If more gain from the circuit is desired, the values of R_6 and R_8 can be changed, but their sum should be kept equal to approximately 50Ω to ensure that the gain of the current-feedback section does not change. In fact, the gain of the input stage can be made as large as 20dB before its bandwidth drops below that of the rest of the amplifier. It is very important to make sure that the 750Ω feedback resistor is an oversized type (at least 2W dissipation rating or greater) since it gets fairly warm during extended periods of high output swing. A low temperature coefficient is also desirable when choosing this resistor since it will minimize the gain change as it heats up.

The references for the two regulator transistors (Q_1 and Q_2) which provide power for the op-amps on board are actually two pairs of standard NPN bipolar transistors used as zener diodes (Q_{14} through Q_{17}). They are connected in series, with their collector leads clipped off, and the net breakdown voltage of each pair is approximately 15V. These devices exhibit significantly less low-frequency noise than the 15V avalanche diodes originally used, and are less expensive as well. They are bypassed with low voltage 10μF tantalum capacitors which filter the noise from the diodes and the power supply rails. Two resistors marked R_{bias} on the circuit diagram, which are connected to each supply rail, serve to bias Q_{14} through Q_{17}. Their values are chosen to provide about 1mA of current in the zener-connected transistors with 40V rails, and the current increases to about 2.4mA with 75V rails. The amplifier chosen for A_1 in this design is a 10MHz gain-bandwidth product BiFET op-amp with a slew rate of 50V/μs, that also exhibits low distortion in the audio band. A_2 is a low-power and low bias-current type with an offset voltage of only 50μV. A_2 must have low offset-current in addition to low offset-voltage because 1MΩ resistors are used, in series with its input pins, to obtain the low integrator crossover frequency. Too large an offset-current would cause additional output offsets due to the differential voltage drop across these resistors.

The two Wilson current mirrors connected to each supply rail, and fed from the collectors of Q_1 and Q_2, are made from a low voltage transistor, a diode and a high voltage transistor (2N5551 or

2N5401). They are degenerated slightly with 100Ω 1% resistors to improve the matching. Anti-saturation diodes (D_2 through D_5) have been included to prevent storage-time problems with the cascode transistors (Q_4 and Q6) in either of the two mirrors during clipping, and this results in excellent overdrive recovery time. Figure 8 shows that the circuit recovers very quickly from overdrive with a 100kHz triangular wave, and no sticking to either power supply rail is evident. The values of the compensation capacitors C_6 and C_7 are 47pF which, when substituted into equation (9) along with the values for R_6, R_7, R_8 and R_{inv} of 16.5Ω, 750Ω, 33.2Ω and 9.13Ω respectively, yield a closed-loop pole frequency of 1.034MHz (A_{buf} was set equal to unity and R_t was assumed to be very large for this calculation). This agrees very well with the measured no-load frequency response of the amplifier plotted in Figure 9, which shows the 3dB point to be very close to 1MHz. The value of R_{inv} used in the calculation of closed-loop bandwidth is actually the open-loop output resistance of A_1 (about 70Ω) divided by one plus the value of its loop gain at 1MHz (about 7.67). This yields the figure of 9.13Ω used.

The output stage bias-voltage generator, connected between the collectors of Q_4 and Q_6, is formed from a programmable zener diode, with an NPN emitter-follower buffer (Q_5) driving its control input. This buffer is not normally required because the bias current of the control input on the zener diode is quite small (a few microamps), but it is included for thermal compensation of the output stage idling current. A common problem with biasing MOSFET output stages is that at moderately low current levels, the decrease in V_{th} of approximately 5 mV/°C causes the drain current to increase for a fixed gate-to-source bias voltage. If, however, the transistor (Q_5) is securely mounted on the same heatsink as the power MOSFET output stage, its V_{be} will decrease as the output transistors heat up. This decrease in V_{be} of about 2mV/°C, which is multiplied up in the bias-generator by approximately a factor three, thus helps to stabilize the quiescent current in the MOSFET output stage. Care must be taken to make sure the wires connecting Q_5 to the amplifier PC board are not excessively long. It was discovered during testing, that when developing high-voltage high frequency squarewaves at the output, the bias-generator voltage tended to decrease only if long interwoven wires were used (greater than a few cm). This caused a reduction in the idling current of the output stage, and presumably was due to the excess capacitance of the leads allowing current to be shunted around Q_5 during the fast edge transitions. An increase in voltage across R_{18} probably resulted from this excess current injection, and the programmable zener diode would have no choice but to react by reducing its anode-to-cathode voltage. In other tests where a high-voltage sinewave or triangular wave was being generated at the output, however, this anomalous behavior did not occur.

Current in the output stage is sensed across two low-value resistors, R_{24} and R_{25}, connected in series with the sources of the power MOSFETs. As the voltage drop across either of these resistors increases towards 0.7V, Q_{12} or Q_{13} will begin to conduct current away from the gain stage and thus limit the output voltage. This is a convenient way to limit the current in the output stage to a safe value. Of course current limiting alone is not enough to guarantee output stage integrity if short circuits to ground at the output are anticipated. This results from the fact that excessive power dissipation in the output stage will still occur if the current limit is too high, even though it may be less than the recommended maximum operating current for the output transistors. Emitter degeneration resistors must be used in conjunction with the two limiter transistors, Q_{12} and Q_{13}, because this circuit has quite a bit of gain when active and tends to oscillate slightly at high

frequencies. Since these transistors must sink or source all the current from the transimpedance stage (up to 30mA) when the output voltage is being limited, the voltage across the 10Ω resistors will increase slightly as the amplifier is driven into hard limiting. This causes a corresponding increase in the actual value of limited current. For the values of R_{24} and R_{25} shown on the schematic diagram (50mΩ) the current limit was about 20A.

A final point worth mentioning is that a larger die-size P-channel power MOSFET was used in the output stage compared to the size of the N-channel device, and was done to equalize the transconductance of each transistor in the crossover region. This results in measurably lower harmonic distortion for a given output stage idling current (250mA was used in this design) since it results in lower open-loop crossover distortion. Because the P-channel MOSFET is larger, its terminal capacitances are also greater than that of the N-channel device. Thus, the two series gate resistors R_{23} and R_{26} are skewed in value to keep the pole frequencies in each half of the output stage approximately equal to each other. The dominant output stage poles, using worst-case capacitance values from the manufacturer's datasheets, are 3.38MHz for the IXTM17P20 P-channel MOSFET and 3.58MHz for the IRF240 N-channel device when loaded by an 8Ω resistor. The HP-41 calculator program listed in [7] was used to determine the pole-zero locations in each MOSFET under these realistic loading conditions.

5. PROTOTYPE PERFORMANCE

Table 1 summarizes the overall performance of the current-feedback power amplifier. Although this design does not achieve astoundingly low levels of harmonic or IM distortion, the measurements made show that the THD and IMD generated by this amplifier are still very low. Figure 10 shows that the THD at 50W output into an 8Ω load is only 0.0017% at 1kHz, and it never rises above 0.01% in the audio band. This is still better than the majority of amplifiers on the market, especially in light of the fact that there is no low-pass LR network in series with output terminal which tends to attenuate high frequency harmonics. SMPTE intermodulation distortion for 60Hz and 7kHz mixed 4:1 is plotted in Figure 11 as a function of level, and it is also quite low, being just above 0.005% at 46W into 8Ω. It should be noted that all distortion tests were performed with a regulated power supply that was current limited to 1A per rail, thus limiting the maximum sinewave power to around 50W.

What does put this topology in a class of its own is the dynamic performance. It has become very trendy to talk about high slew-rate in reference to audio power amplifiers, but proper wavefrom control during reproduction of a squarewave is just as important. Although few applications would probably require any audio amplifier to reproduce high-frequency squarewaves, since it would likely result in the destruction of high-frequency transducers, this design is capable of accurately reproducing a squarewave when required. Consequently, the value measured for DIM-100 dynamic intermodulation distortion is a very low 0.0015% at 46W output into 8Ω, as shown in figure 12. The large signal step response of the amplifier with no load is shown in Figure 13, and a small amount of overshoot is visible here on the rising edge of the waveform. This occured because A_1 was driven into current limiting during the time the compensation capacitors were be-

ing charged. Slew-rate limiting, which is observed in the transimpedance stage at about 220V/μs, is a consequence of the current limiting circuitry built into A_1, and with most of the op-amps tested it was less in the positive direction than the negative. When lower amplitude squarewaves are being generated (< $90V_{p-p}$), the positive edge overshoot does not occur, but Figure 14 indicates that the circuit is still very well behaved with a 100kHz 100Vp-p squarewave at the output.

6. CONCLUSION

The current-feedback power audio amplifier presented in this paper is quite unlike its voltage feedback predecessors, because it allows very high performance to be achieved with just a single gain stage. Ultra-low static distortion figures have not been obtained with this design; however, the distortion is still acceptably low and has not proven to be audible. The dynamic performance of this topology is what sets it apart from other designs of comparable complexity, and indeed many commercial amplifier designs could benefit from the ideas expounded here.

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[6]. Derek F. Bowers, "A Precision Dual "Current Feedback" Operational Amplifier", Proceedings of the Bipolar Circuits and Tech. Mtg., pp. 68-70, September 1988.

[7]. Mark Alexander, "Frequency Response Analysis of the MOSFET Source Follower", Application Note AN83-8, Siliconix incorporated, November 1983.

SUMMARY OF AMPLIFIER PERFORMANCE

Power Output (supply limited):	50W ($R_L = 8\Omega$)
Total Harmonic Distortion at 1kHz:	0.0017% at 50W
Total Harmonic Distortion at 20kHz:	0.01% at 50W
SMPTE Intermodulation Distortion:	0.005% at 46W
Dynamic Intermodulation Distortion (DIM-100):	0.0015% at 46W
Frequency Response:	DC to 1MHz
Slew Rate:	>200V/μs
Risetime (input filter in circuit):	400ns
Total Quiescent Supply Current:	300mA

Table 1: Summary of amplifier performance

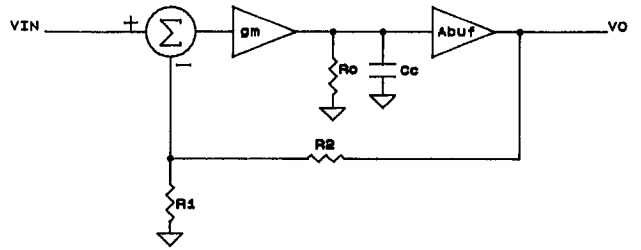

Figure 1: This simple model for a voltage-feedback amplifer includes the basic building blocks common to most op-amps, and is adequate for analysis.

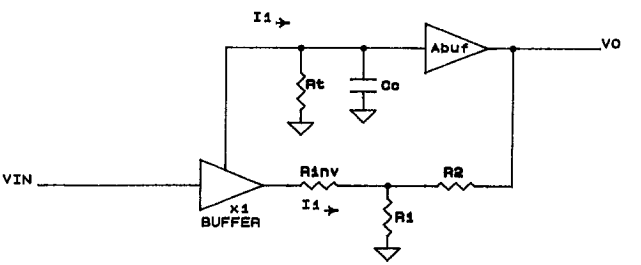

Figure 2: The model of a current-feedback amplifier is quite different from that of figure 1, because an error current I_1 determines the ouput voltage.

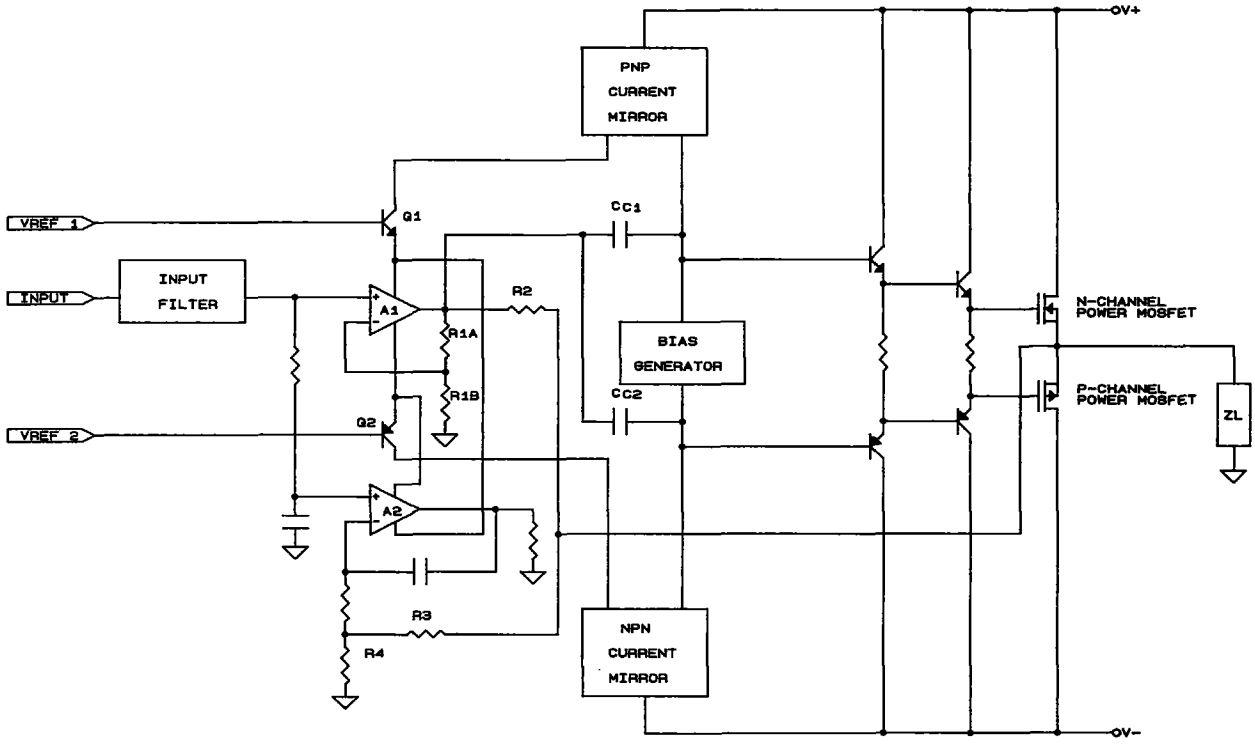

Figure 3: The simplified block diagram of the amplifier shows that an op-amp is used as the input buffer and thus can be used to provide some additional gain. A second op-amp is used to provide accurate DC amplification independent of the main current-feedback loop.

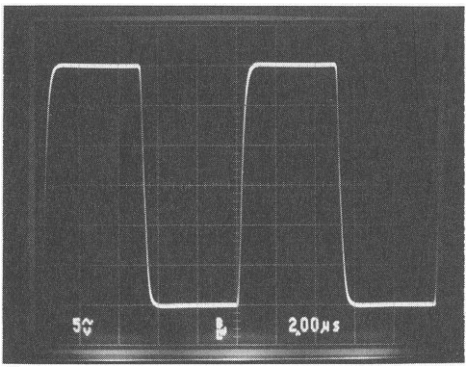

Figure 4a: The no-load squarewave response shows little sign of instability, when 100pF compensation capacitors connected to ground are used.

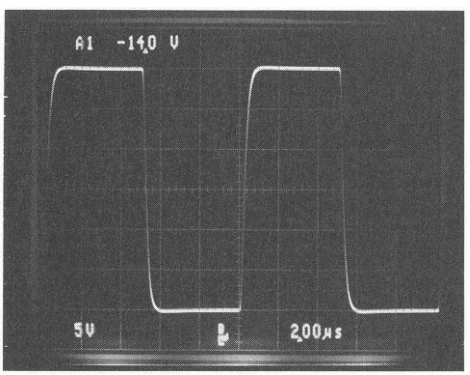

Figure 4b: The no-load response to a squarewave, when 47pF compensation capacitors connected to the summing node are used, is also quite well behaved.

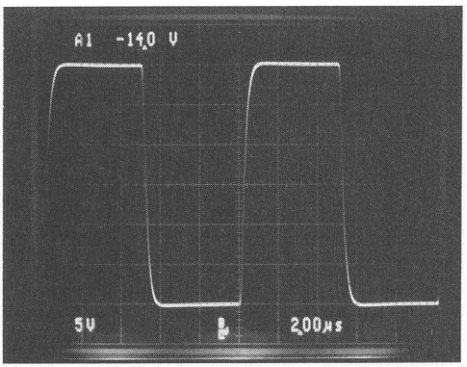

Figure 5a: The loaded squarewave response shows instability on the negative edge, when 100pF compensation capacitors connected to ground are used.

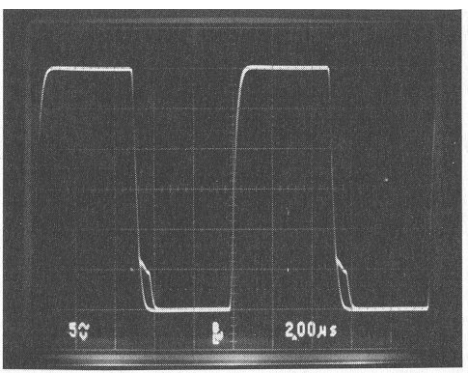

Figure 5b: The loaded response to a squarewave, when 47pF compensation capacitors connected to the summing node are used, does not indicate any instability.

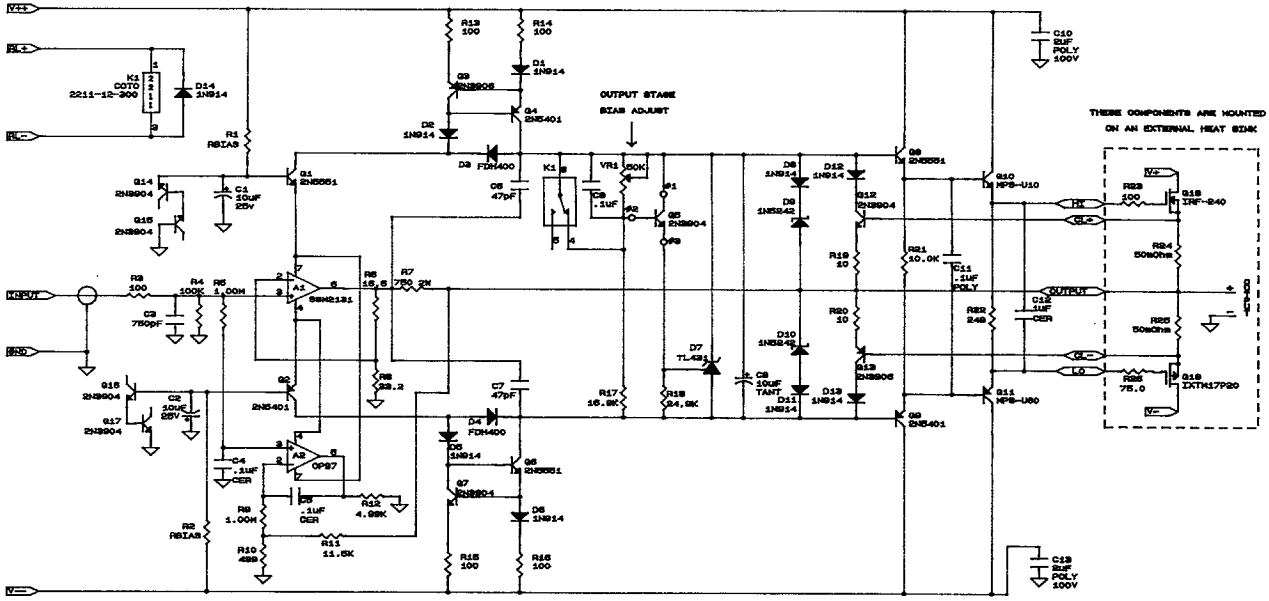

Figure 6: The circuit diagram of the amplifier shows that two op-amps are used to minimize the overall cost and component count.

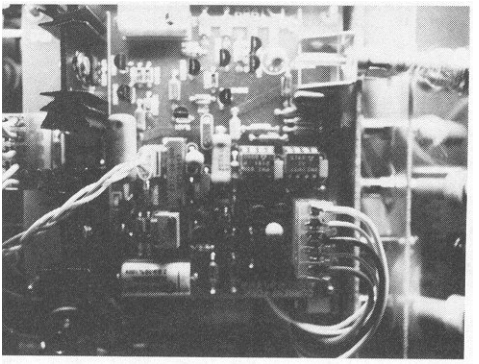

Figure 7: The entire power amplifier circuit, less the output transistors, fits easily onto a PC board that measures about 9x9 cm.

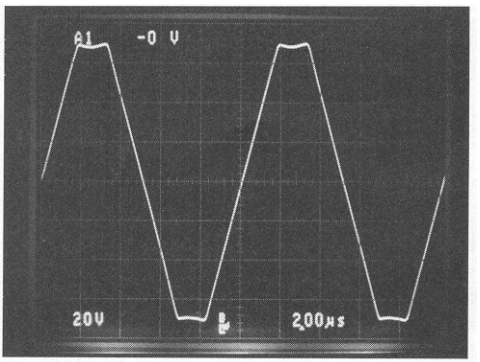

Figure 8: The clipping behavior of the circuit with a 100kHz triangular wave shows no unusual transients or sticking to either power supply rail.

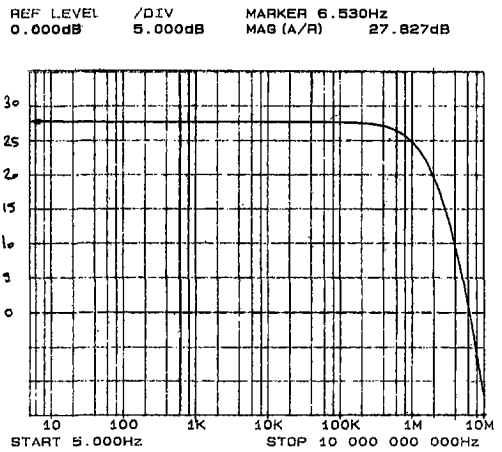

Figure 9: The frequency response of this topology shows no sign of any peaking, and is down approximately 3dB at 1MHz.

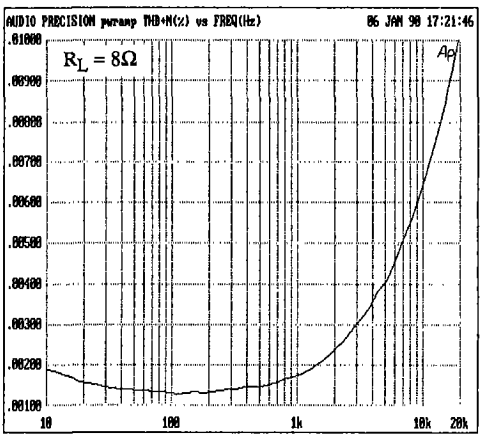

Figure 10: The THD of the amplifier is below 0.01% at all frequencies in the audio band when delivering 50W to an 8Ω load.

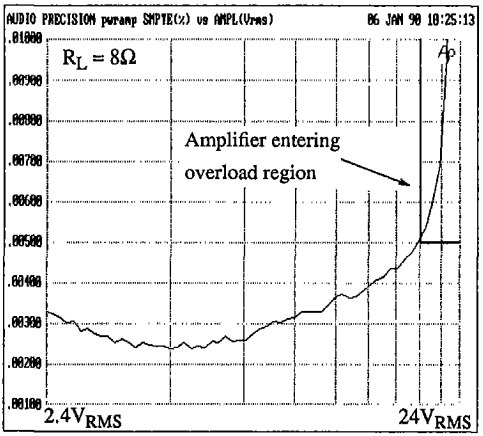

Figure 11: This plot of SMPTE IMD for 60Hz and 7kHz mixed 4:1 shows relatively little change as the power output level is increased.

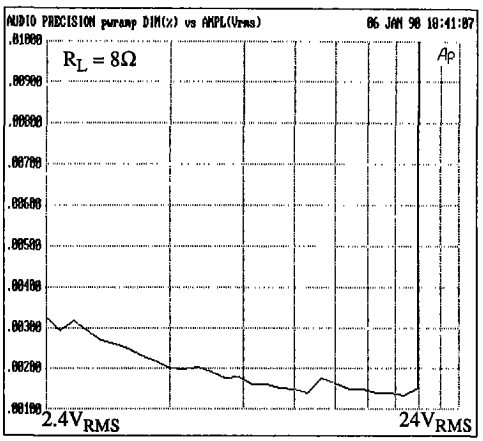

Figure 12: The DIM-100 distortion curve for this amplifier is very low, and is a direct consequence of its clean transient response.

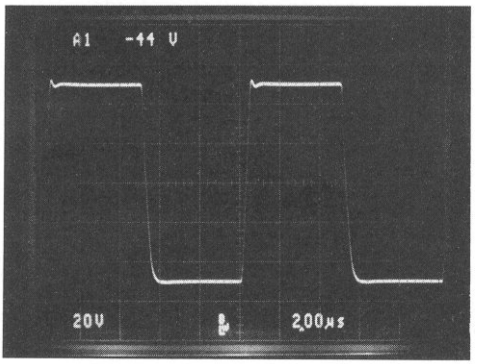

Figure 13: The step response at the output, with no load connected, shows very minimal overshoot and t_r is about 400ns.

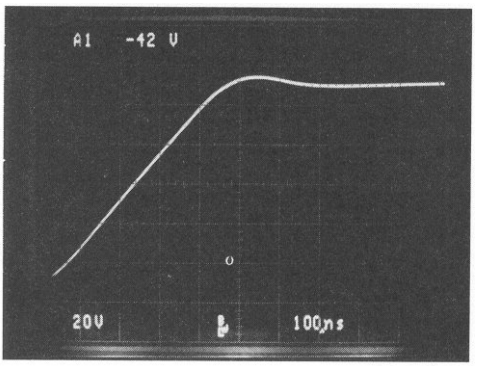

Figure 14: A 100kHz 100Vp-p squarewave is reproduced without any difficulty, but it is not something every amplifier can do.