Two Novel Cross-Cascode Differential Amplifiers

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Abstract – Two novel cascode circuits, the Differential Cross-Cascode and Differential Cross-Follower, is proposed and investigated. Its fundamental distinction from the Differential Ordinary Cascode consists in the input signal voltage being applied simultaneously to the inputs of common emitter/source and common base/gate stages, and besides the inputs of CE/CS and CB/CG being cross-coupled. We show that the input signal is amplified in the input circuit, furthermore the input impedance and the current gain increase considerably and the bandwidth is essentially expanded. Simulation results of such a cascode designed with IBM BJT and FET transistors are presented. The actually obtained bandwidths (BJT-18.7 GHz, FET-7.8 GHz) proved as predicted to be more than twice as wide as compared with the bandwidth of the ordinary cascode (BJT-8.6 GHz, FET-3.4 GHz).

Key – Words: - Cascode, emitter-follower, cross-connected cascode, cross-coupled cascode, differential amplifier.

1 Introduction

One of the most efficient and frequently used circuits, favoring enhancement of the features of the main amplifying stages is the cascode circuit, i.e. common emitter/source-common base/gate (CE/CS-CB/CG) connections. Further on, we shall call this circuit Differential Ordinary Cascode (DOC) and for clarity's sake we will consider only its BJT-based type. The uncountable number of papers dealt with its investigation and different applications. However, research work continues to appear and new application opportunities are proposed.

A rather full presentation of the properties of the ordinary cascode circuit is given, for instance in [1]. But this simple configuration does not allow increasing cascode current gain, input and output impedances and frequency band of the circuit as compared to the standard CE cell. The main cause is feeding of the input signal to the base of the CE stage only.

A great number of inventions and scientific research work has been dedicated to overcoming the drawbacks and limitations of the standard cascode and developing its merits. Let us mention at first the original patent [2], which proposed to use input matched resistors cross-coupled between the bases of the CE and emitters of the CB cascades to increase gain and dynamic range. Then denote the work [3], which proposes to apply a negative feedback between emitter and base of the CB stage by means of a dedicated amplifier in order to considerably increase the output resistance of the cascode. Finally, the urge increase of allowable output voltage, power, efficiency and enhanced matching with the load has lead to the creation of various multistage cascodes [4] made up of a CE stage and several CB stages. Important improving was made in [5]. It was proposed to place load resistance between emitters of the CB cascades and to drive their bases by the two complementary outputs of the differential signals.

This brief overview is aimed to show that a signal additionally applied to the base of a CB stage may considerably increase the output impedance and output voltage of the circuit and somewhat improve the circuit parameters, but does not permit of changing appreciably its transfer function and input resistance. This is quite natural, because the characteristics of the CE stage remain unchanged.

Using regularly the cascode in its differential form, we paid attention to some of its fundamental features, which allow improving the basic characteristics of the circuit. We will describe the qualitative features of the two novel circuits, analyze them theoretically, and compare it with the standard cascode. We will also present a few results of the development of Fet-based cascode with a bandwidth 7.8 GHz.

2 Fundamental

In the framework of this paper we will study differential two such-like cascode configurations, i. e. series connected CE/CS or CB/CG cascades intended to convert the input voltage into output voltage or current. We will show that feeding in-phase signal current to emitters of the CB/CG stages and simultaneously the anti-phase input voltage signal to its bases permits of:

- increasing the current gain,
- expanding the bandwidth of the amplified signals,
- modifying, specifically, diminishing the input admittance.

Strictly speaking, such circuits are no longer a cascode, i. e. a combination of CE-CB stages. Nevertheless, it seems rational to keep this term and, therefore, we call these devices hereinafter Differential Cross-Cascode (DCC) and Differential Cross-Follower (DCF). Its functional circuits are shown in Figs.1(a) and (b).

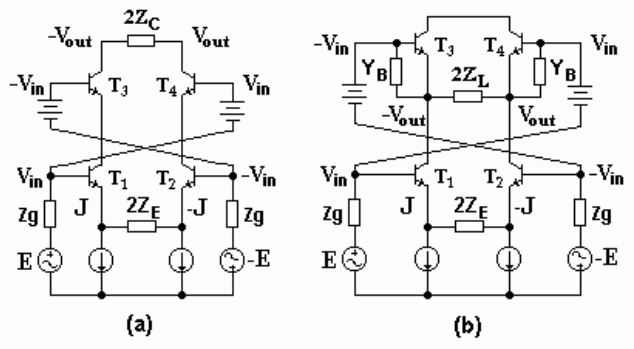

Fig.1 (a) – DCC cascode, (b) – DCF cascode

Let us explain how works e.g. DCC amplifier. The transistors T_1 and T_2 are connected in a CE-configuration. Transistors T_3 and T_4 –

are in CB configuration. The transistors T_1 and T_3, as well as T_2 and T_4 are connected in series to form two cascodes. The bases T_1 and T_4, T_2 and T_3 are interconnected and form a DCC cascode. The differential input voltages Vin and -Vin are applied to the bases T_1 and T_2 and generate the currents J and -J, which are injected into the emitters of transistors T_3 и T_4. The same input voltages are applied to the bases T_4 and T_3. The base voltages and the base currents of the CB stages are approximately opposite by phase (at low frequency approximation) and are, therefore, perceived by the input voltage sources as negative load impedances. That is why, the base currents of the CB transistors that are equal to $J\alpha_1(1 - \alpha_2)$ are flowing back to the bases of the CE transistors and are subtracted from the CE base currents $J(1-\alpha_1)$. As a result, the total input current of the circuit is decreased to the amount of $J(1-2\alpha_1+\alpha_1\alpha_2)$ thus decreasing the cascode input current and its input admittance. In our formulas α_1, α_2 are the collector-emitter current gain for CE and CB transistors accordingly, and J is the emitter current of the CE stage. A more accurate analysis and simulations with account for the relationship α as a function of frequency and time delay show that the real part of the input admittance is getting negative. The imaginary (capacitive) part is getting much smaller in a broad band of frequency. It can be shown that owing to this phenomenon the magnitude of the input voltage at the inputs of the cross-connected circuit grows at frequencies close to the transistor's maximum operating frequency. As a result, the bandwidth of the circuit can be doubled and the total frequency response flatness is improved. Alike qualitative explanation valid for DCF circuit if $G_L=Y_B= 0$. If $G_L> 0$ base currents of the CB cascades are decreasing. To compensate input currents of the CE cascades in this case we use additional Y_B conductance.

We would like to stress that although we describe circuits using BJT parameters only, majority of conclusions are valid for cascodes made of any other amplifying elements as well.

3 Analysis

3.1 The equivalent circuit and restriction

The goal of our theoretical analysis is to investigate the most important phenomenological features of the novel circuits, but in no way to compare in details the theory with the experimental data. That is why; we used the simplest equivalent transistor circuits and, sometimes, even excluded from the cascode circuit some components, which, although important for its normal functioning, are of minor importance for the analysis of its fundamental features. We used also standard p-type models for the transistors. Formally, these models are suitable for the majority of transistor types. This simple model includes: transconductance Gm, input, output and transient conductances *Yp, Yo* and *Yf*. The differential form and cross-connection of the cascode were reflected by introducing an ideal input signal phase inverter for the CB stage.

First of all, we will investigate the DCC and DCF cascodes itself and only afterwards its input circuit. To do this we have to establish beforehand some general rules and restrictions.

- All conductances (resistances) are dimensionless values, normalized on Gm_{CE} – transconductance CE, so $Gm_{CE} = 1$. However, for convenience's sake, 1 when interpreting the formulae does not replace the parameter Gm_{CE}.
- In most cases the exact solutions of equations don't have great practical importance, because the transistor model is represented in a simplified form. We assume input, transient and output conductances $|Yp|$, $|Yf|$, $|Yo| \ll 1$ and $|Yf|$, $|Yo| < |Yp|$ at all frequencies within the bandwidth of the amplifier.

3.2 Cascodes with idealized non-identical transistors

Let us consider the simplest DCC and DCF cascodes made up of idealized but not an identical transistors with $Yp_{CE} \neq Yp_{CB} \neq 0$, $Yf = Yo = Ze = 0$. The exact solutions are given in Eqs.1, 2 and 3.

$$Yin = \frac{Yp_{CE}\left(G_L + Gm_{CB}\right) + Yp_{CB}\left(G_L - Gm_{CE} + Yp_{CE}\right)}{\left(G_L + Gm_{CB} + Yp_{CB}\right)} \quad (1)$$

$$Vout_{DCC} = -Vin \bullet Z_C \bullet \frac{Gm_{CB}\left(Gm_{CE} - G_L\right)}{\left(G_L + Gm_{CB} + Yp_{CB}\right)} \quad (2)$$

$$Vout_{DCF} = -Vin \bullet \frac{\left(Gm_{CE} + Gm_{CB} + Yp_{CB}\right)}{\left(G_L + Gm_{CB} + Yp_{CB}\right)} \quad (3)$$

Here and hereinafter $G_L = Z_L^{-1}$; (1) is valid for both DCC and DCF cascode configurations; (2) refers to Fig.1 and (3) – to Fig.2 cascode configurations. Note that ordinary for DCC in (2) $G_L \approx 0$.

Let consider the input current and, therefore, the input conductance of the DCC and DCF cascodes, which makes their major distinction from the regular cascode. It follows from the circuit and from the relation (1) as well that the input current represents formally the difference of the two base currents of the transistors CE and CB respectively. However, since the current gain of the cascode is a multiplicative process, the cascode input current contains in fact additive and multiplicative components and this peculiarity is extremely important. The additive components are in opposition and in case of identical transistors they cancel one another for. This provides wide opportunities in controlling the input impedance. In turn, the multiplicative components allow, for instance, conversing reactive components into active ones. We have to point out that the hereinafter-discussed possibilities to control the frequency dependence of the input conductance in the neighborhood of the bandwidth boundaries are of crucial importance for solving the problem of expanding the DCC and DCF cascodes bandwidth. Said is valid for both types of cascodes. So, to simplify analysis and formulas farther we shall investigate DCC and DCF configurations only for $G_L = 0$ and for identical transistors.

We assume $Yp \approx i \cdot x \cdot Gm$, where x is a certain relative frequency and x ~ 1 correspond to a frequency close to the limit one. This, of course, refers to BJT and CMOS transistors as well. Then, from (1) the dependence of the input conductance upon the relative frequency *x* becomes a very simple one

$$Y_{DCC}(x) = Y_{DCF}(x) = -Gmx^2(1+ix)^{-1}[1+Te(1+ix)]^{-1} \quad (4)$$

$$Y_{DOC}(x) = ixGm[1+Te(1+ix)]^{-1} \quad (5)$$

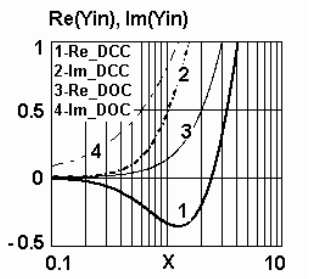

Fig.2 Frequency dependencies of the input conductance of DOC and DCC/DCF cascodes: Gm = 1, Te = 0.2.

Here and hereinafter *Te = GmZe, Tg = GmZg*. The fundamental distinction between of cascodes is shown in Fig.2 representing the characteristic dependences of the real component of the input conductance - curves (1) and (2) - and of its imaginary component - curves (3) and (4) – for DCC and DOC cascode types. Here and hereinafter curves represented on the respective figures are marked in the text as type-"(3)".

There are two major features: a considerable reduction of the input conductance and a negative real component of the conductance in the amplifier bandwidth. The last feature is linked to the conversion of the purely imaginary (capacitive) conductance into negative real conductance. The dependence of this real component upon the frequency is quadratic but at high frequencies (x ≈ 1) and for Te > 0 it has minimum and then increases.

Let us emphasize that the transconductance *G(x)* of the DCC and DOC cascodes is described by the single relationship (6).

$$G(x) = Gm(1+ix)^{-1}[1+Te(1+ix)]^{-1} \qquad (6)$$

3.3 Total transfer function

The total transfer function of the cascode is the product of the transfer function of cascode itself and transfers function of its input circuit. For the same case of identical ideal transistors *Yp = i·x·Gm, Yf = Yo = G_L = 0.*

$$G_{DCC}(x) = \frac{GmZc}{1+Te+ix(2Te+1)-x^2(Tg+Te)} \qquad (7)$$

$$G_{DCF}(x) = \frac{2+Te+ix(2Te+1)-x^2Te}{1+Te+ix(2Te+1)-x^2(Tg+Te)} \qquad (8)$$

The module (7) and (8) is of primary interest. The squared denominator is a polynomial of the 4th order in x. With a predetermined deviation from 1 the optimum transfer function is expressed either by the Butterworth polynomial, or by the Chebyshev polynomial.

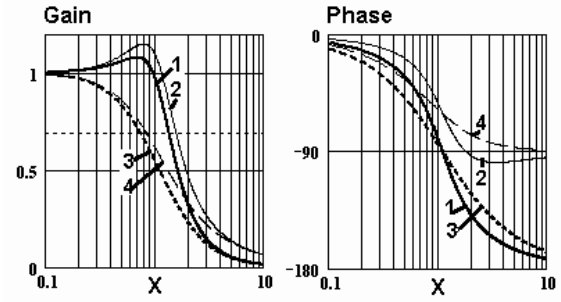

Fig.3 Transfer functions of DCC-(1), DCF-(2) and DOC-(3 and 4) cascodes: Te = 0, Tg = 1.

Fig.3 shows module and phase of the normalized transfer functions (7) and (8), where curves (1) and (2) relate to the cross-connected cascodes and curves (3), (4) to the regular cascodes without cross-connection, herewith curves (1) and (3) relate to the output of Fig.1a and curves (2) and (3) relate to the output of Fig. 1b schematics. Comparison -3dB bandwidth of cross-connected (1), (2) and regular (3), (4) cascodes shows broadening in two times approximately.

The cause of such an important broadening of the bandwidth at the same transfer function of the cascode itself (6) is evident. At the input of the regular cascode the signal is attenuated owing to the effect of the input capacitive conductance of the CE/CS stages. And on the contrary, the signal is amplified at the input of the DCC/DCF cascodes at high frequencies due to the effect of the negative real component of the input conductance (1).

4 Simulation

We have designed and tested several modifications of the cascode circuit using BJT and FET transistors. The work was aimed to verify the increase of the input impedance, current gain and bandwidth of the DCC and DCF cascodes predicted by the approximation theory as compared to the DOC cascode. Here we present data on FET-based circuit. Schematic data and simulation results of the BJT-based DCC cascode were quoted in [7].

In the framework of this study we were intended to minimize the side effects and the influence of secondary factors affecting the investigation results and the circuit comparison, and also to simplify as far as possible the description of the actually used circuits. In this connection simulation has been limited to the most simple cascode circuits Figs.1a and b. The dc voltage and current sources are ideal ones. The values of currents, voltages and main components of the circuit and FET transistors are shown in the Table 1. The main parameters of DCC and DOC cascodes designed in IBM SiGe CMOS technology are given in the table as well.

Table 1

	$T_1...T_4$ μ	Zg Ω	Ze Ω	Zc Ω
DCC	28x0.2	500	1	305
DOC	28x0.2	500	1	290
	Io mA	Vcc V	Go dB	BW G
DCC	2.2	3.2	13.8	7.8
DOC	2.2	3.1	13.8	3.4

We describe and briefly discuss the simulation results obtained using the CADENCE simulator. They presented on Fig.4.

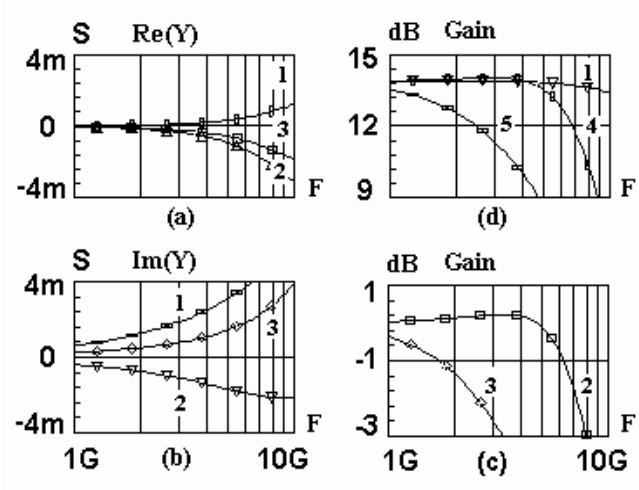

Fig.4 CMOS-based DCC and DOC cascodes. Simulation results (see description in the text): (a) and (b) – cascodes input conductance; (c) – transfer functions of the input circuit and (d) - transfer functions of the cascodes.

4.1 Input conductance

Fig.4 shows the dependence upon frequency of the real (a) and imaginary (b) components of the transistor input conductances CS (1) and CG (2) and also their sum (3) – that is, the input conductance of the DCC cascode. In full concordance with the analysis given before CG (2) transistor conductance is negative

resulting in a dramatic reduction both components of the cascode input conductance. If the transistors are identical, the real component of the input conductance is always negative within the bandwidth since the delay causes the capacitive component to convert into negative active component.

4.2 Frequency response

The various Gain transfer functions of the cascodes – the main characteristics of any amplifier – are given in Figs.4c, and d. As pointed out before, the voltage transfer function (6) of the cascode itself is identical for both of the circuits. Its bandwidth (curve (1)) makes 27 GHz. The bandwidth of the voltage transfer functions of the input circuits DCC (curve(2)) and DOC (curve(3)) cascodes make 8 and 3.2 GHz respectively, in full compliance with the formerly carried out analysis (see, e.g. Fig.3 curve (1)). The first one shows a maximum 0.4 dB at the frequency of 4 GHz. As a result, the voltage transfer functions of the DCC (curve (4)) and DOC (curve (5)) cascodes have a bandwidth of 7.8 GHz and 3.4 GHz respectively. Besides, a more rectangular shape is inherent to the function (4). Therefore in a multistage DCC cascode amplifier the bandwidth will be decrease very slowly.

4.3 Current gain

The current gain β of both cascodes are shown in Fig.5 and they relate to BJT – based schematic [7] . It is evident that β_{DCC} is high and amounts to $\beta_{DCC} \cong \beta_{DOC}^2$ (β_{DCC} - (1), β_{DOC} - (2)) up to ~1 GHz. Further, $\beta_{DCC} < \beta_{DOC}^2$ and this inequality builds up with frequency.

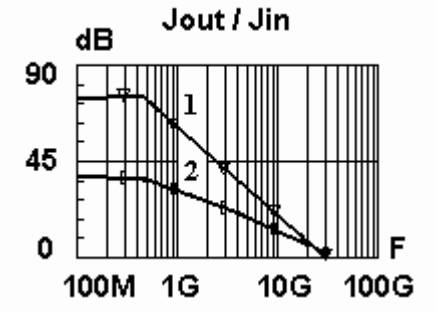

Fig.5 Current gain of BJT-based DCC (1) and DOC (2) cascodes.

Obviously this is connected with the effect of the output and transient collector-base impedances, which differ in each of the cascodes.

5 Conclusions

The frequency dependences of the input impedances and transfer functions inherent to these circuits have proven to coincide and the approximately twofold bandwidth expansion and the considerable increase of the current gain and input impedance predicted by the theory have been confirmed.

Owing to these features the DCC and DCF cascodes provide essentially better parameters as compared to the regular cascodes [6,7] in all circuits implemented in our development work using BJT and CMOS transistors.

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