Service information for 67cd dac/supply board.

POWER SUPPLY:

Mains are applied to the board via H1 (Neutral), H2 (Live) and H3 (Earth) and is, to obtain EMC, filtered prior to mains voltage selection.

For 220V/240V operation:

Link PLM1 to PLM3

For 110V/120V operation:

Link PLM1 to PLM2 and
PLM3 to PLM4

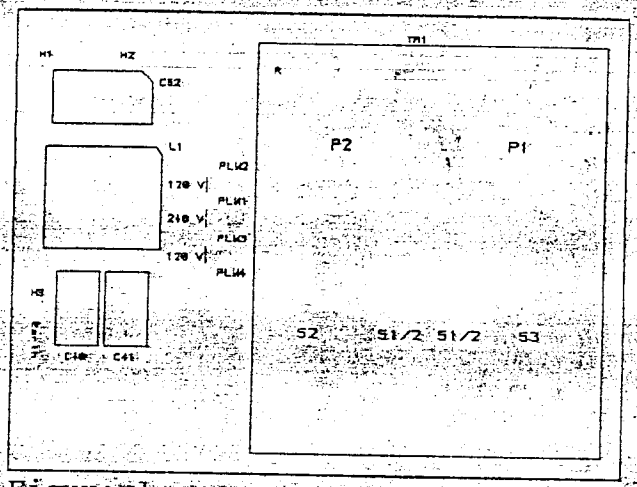


Figure 1

The 67cd uses a 24 VA low profile transformer with 3 secondary windings (1 Digital and 2 analogue).
Linear regulators provides 7 power rails:

	NAME	VOLTAGE	NOMINAL CURRENT
Digital	"+5V"	: +5.0V	450 mA
Diskdrive	"+Vm"	: +8.8V	110 mA
	"-Vm"	: -8.4V	80 mA
Analogue	"+VA1"	: +5.0V	60 mA
	"-VA1"	: -5.0V	60 mA
	"+VA2"	: +9.0V	10 mA
	"-VA2"	: -9.0V	10 mA

The following diagram (fig. 2) shows the power supply.

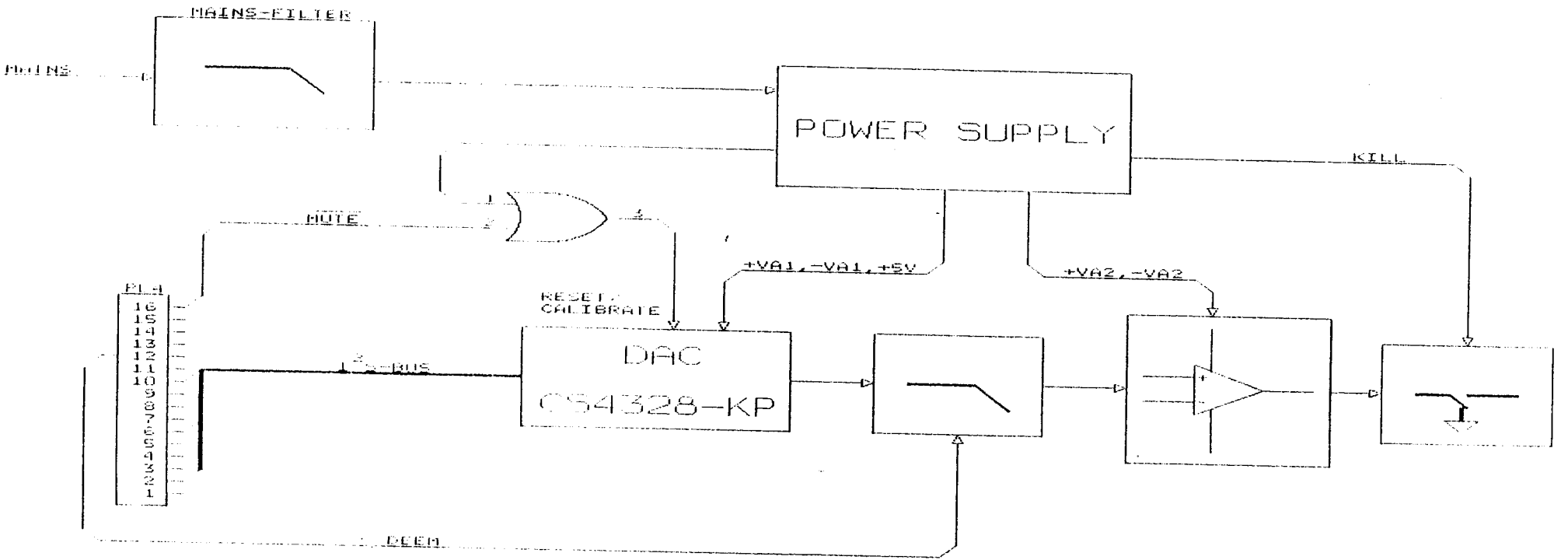

MAINS-FILTER
MAINS
POWER SUPPLY
KILL
MUTE
+VA1,-VA1,+5V
+VA2,-VA2
RESET/
CALIBRATE
DAC
CS4328-KP
DEEM

Figure 3

DIGITAL TO ANALOG CONVERSION:

The DAC (CS4328-KP) is via PL4 feed digital audio, in I^2S format ,from the decoder board (3104 113 3027):

I^2S comprises of 4 signals:

XTI: Master clock 11.2896 MHz.

LRCK: Left right clock 44.1 KHz.

SDATAI: 18 bit (16 bit followed by 2 zeros) serial data. The 16 bit is represented in 2's-complement format MSB first.

BICK: Serial bit Clock for SDATAI 2.8224 MHz. (Clocks in the individual bits of the serial data).

The block diagram fig. 3 shows the general signal paths on the dac/supply board.

The DAC delivers an analog output voltage with a full scale equivalent of 2 V_{peak}. This signal is passed through a filter section which consists of a 1'st order lowpass filter (f_{3db}=100 KHz) to remove any spurious products left over from the D/A process,plus a de-emphasis facility, which action is controlled by the pre-emphasis flag on the disc being played. The following op-amp stage amplifies the signal to the recommended full scale equivalent of 2 V_{rms} (A_7=1.41).
Prior to the output connectors is a muting (KILL) circuit which shorts the output to ground during power up and power down.

The DAC has a reset/calibration (/RST) input which is an active low signal that resets the DAC's digital filter and delta sigma modulator plus performs an offset calibration of the output. When /RTS is active the analog outputstage is muted. /RST is held low during power up or power down conditions and also when no digital audio is present (when the player has no disc inserted, and when in stop, skip or pause mode).

67CD POWER-SUPPLY

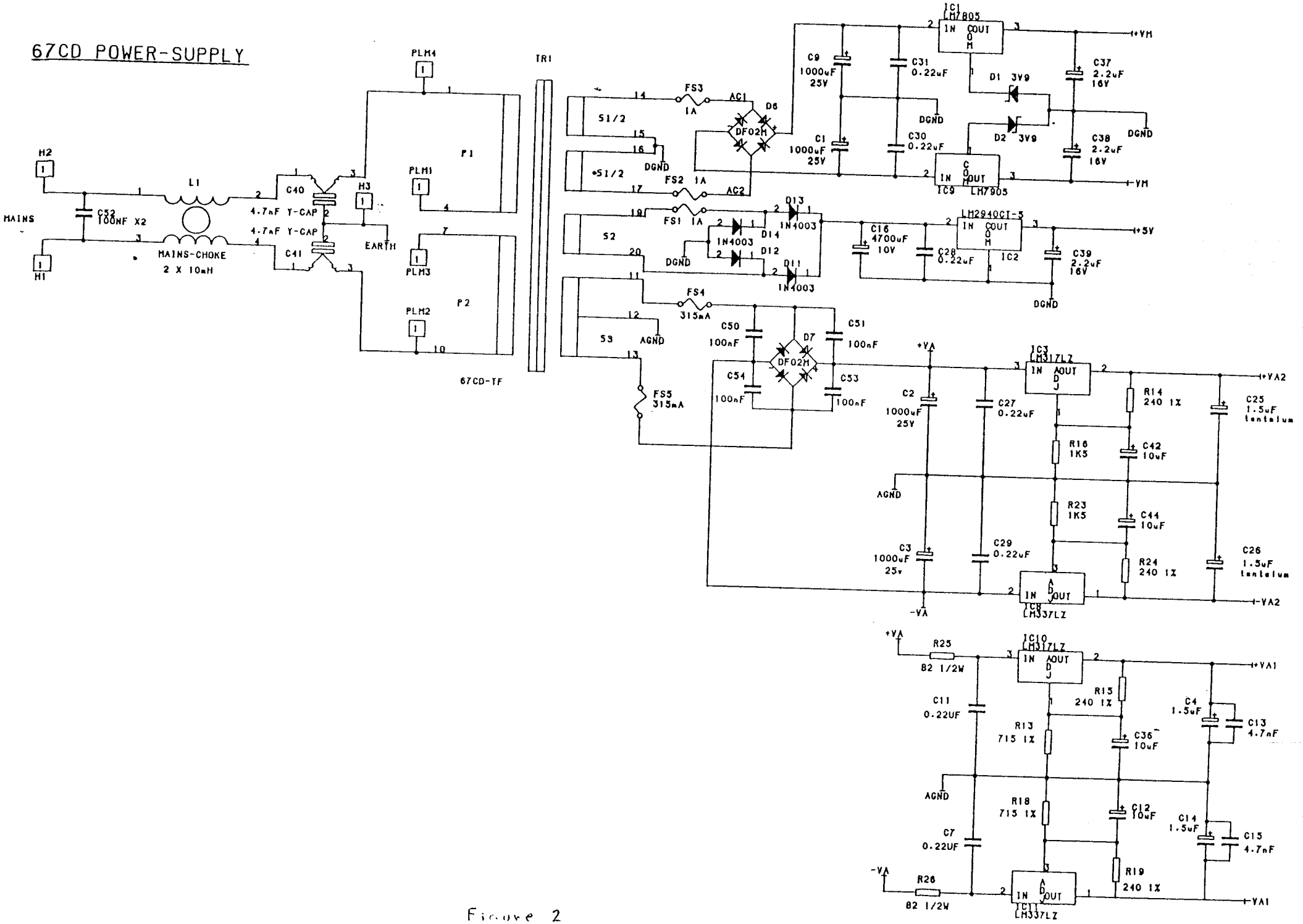


Figure 2

CRYSTAL CS4328-KP:

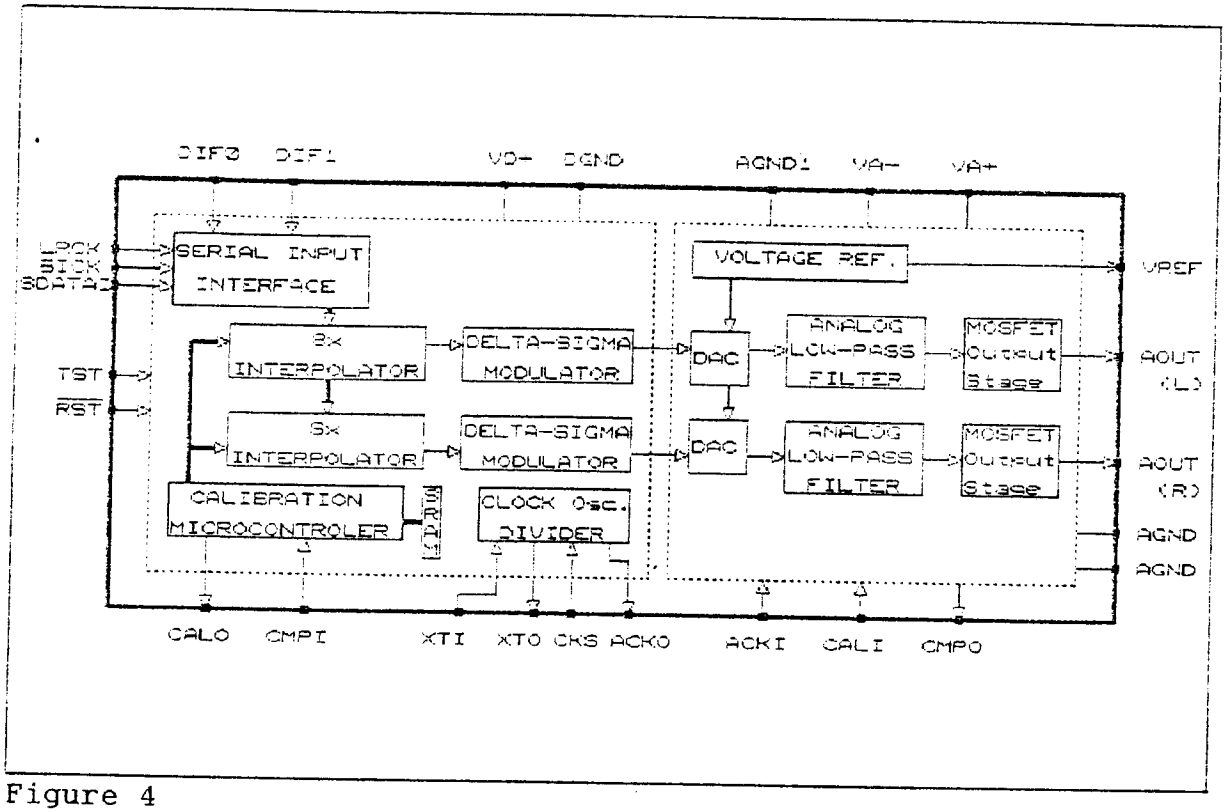
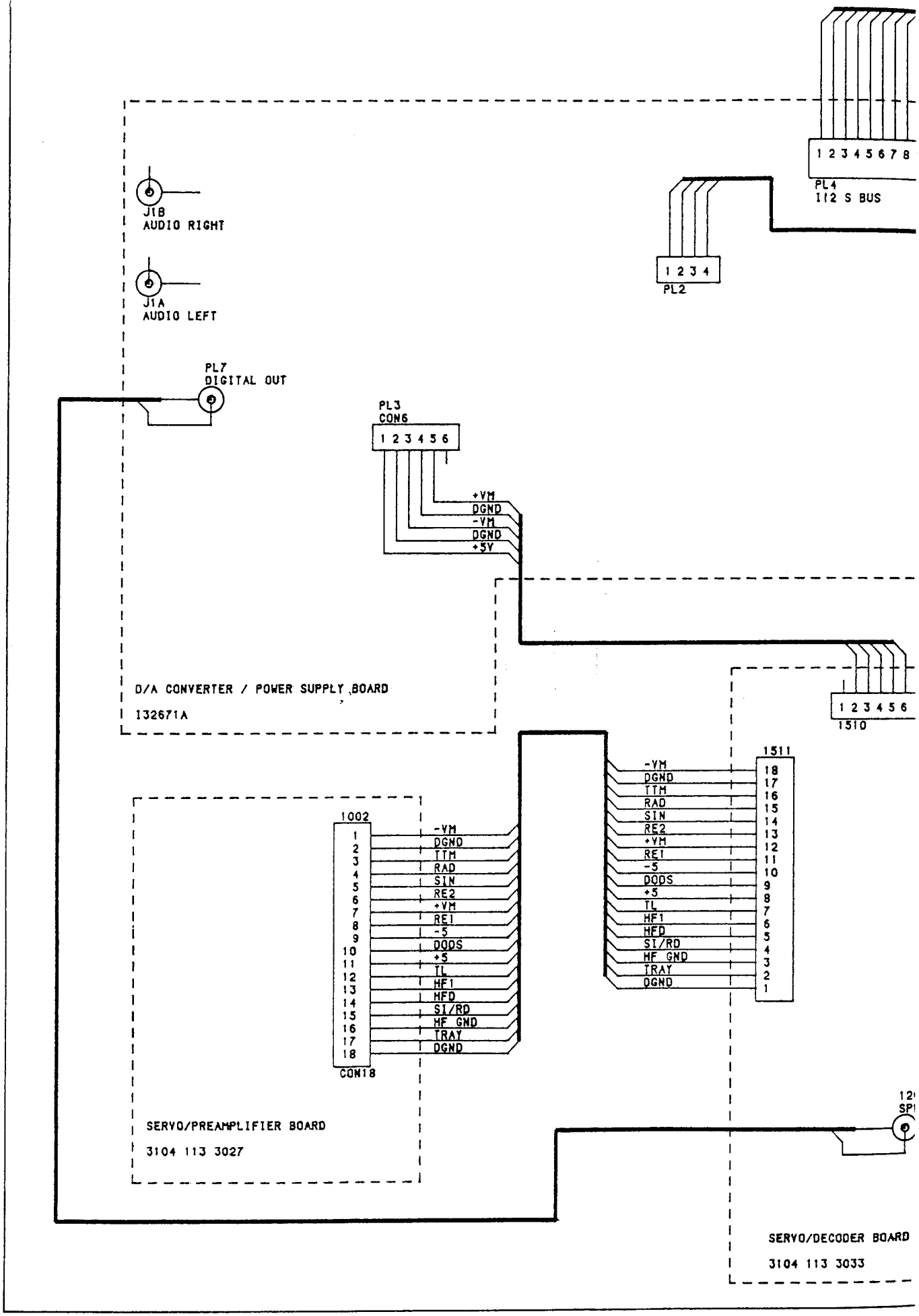
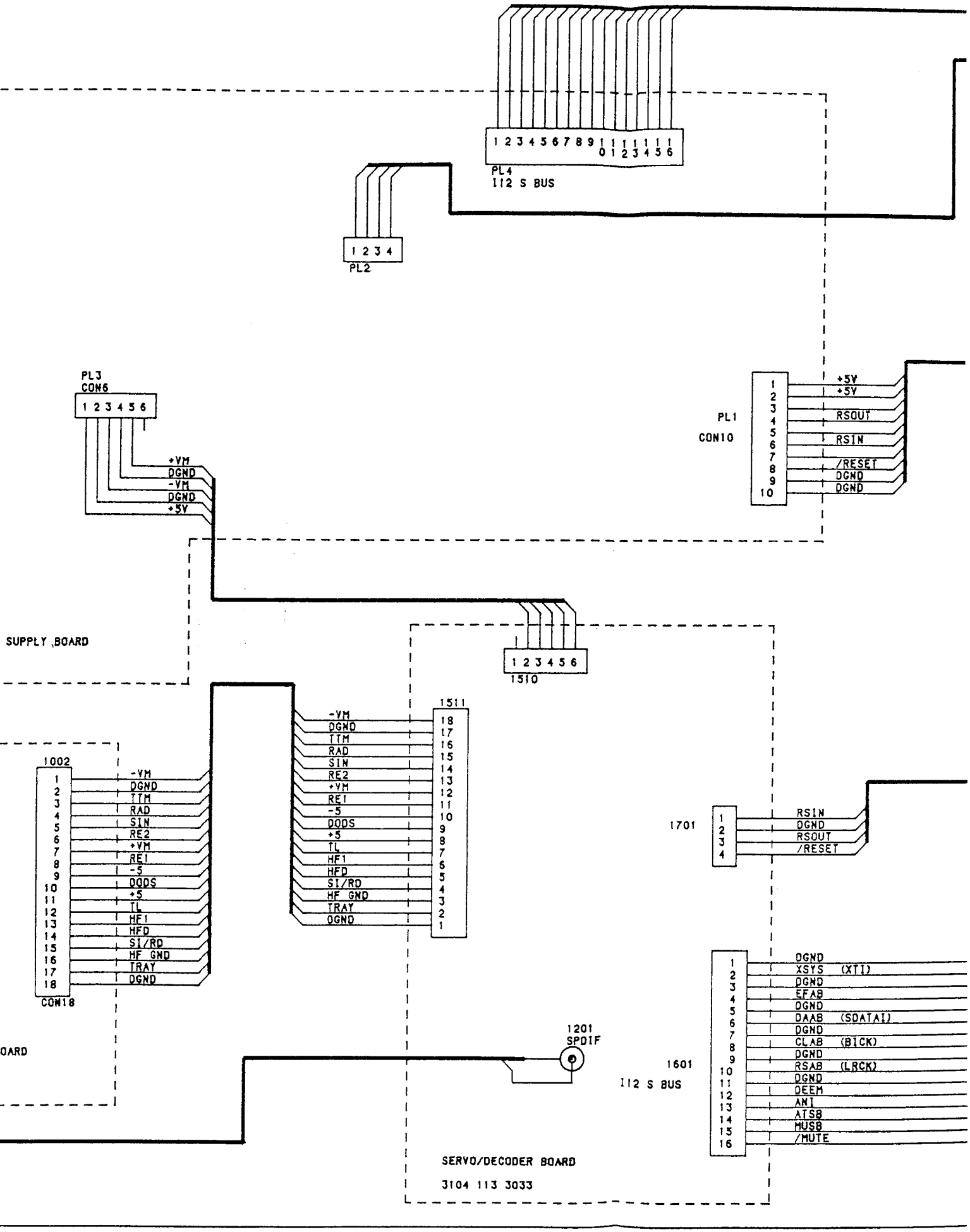
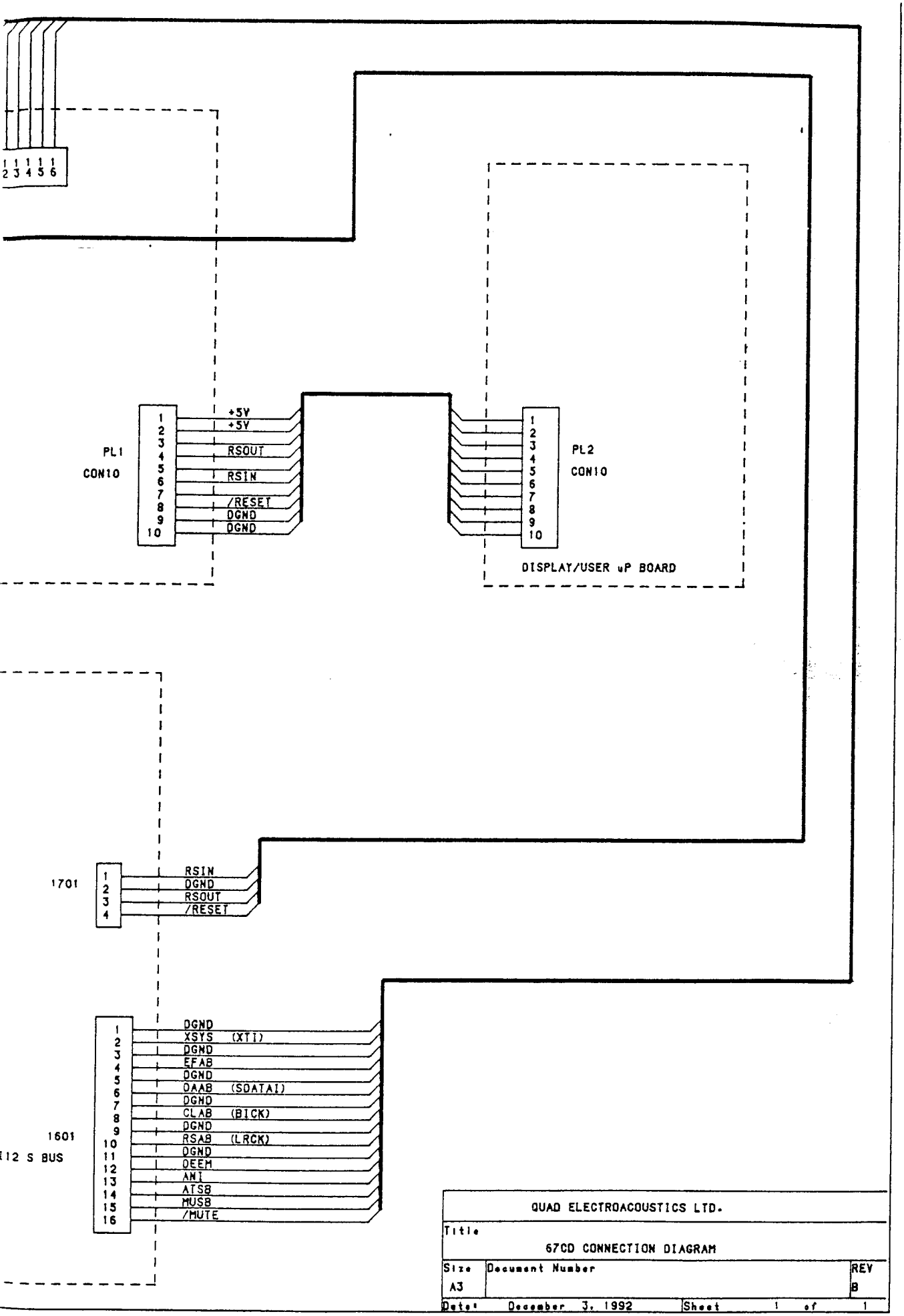


Figure 4

The CS4328 is oversampling the input signal 64 times by means of interpolation (8x) and digital sample and hold (8x).
The oversampled signal is then translated into a bitstream via an Delta-Sigma modulator (5th order noise shaper) for which output it applies, that the density of the 1's is proportional to the magnitude of the desired analog signal. The modulator is followed by a D-to-A converter that transform the 1-bit signal into a series of charge packets. The magnitude of the charge in each packet is determined by sampling of a voltage reference onto a switched capacitor, where the polarity of each packet is controlled by the 1-bit signal. The final stage of the cs4328 is made up of a 5th order switch-capacitor low pass filter and a 2nd order continuous time filter. The switched-capacitor filter eliminates out of band energy resulting from the noise shaping process. And 2nd order continuous time filter removes sampling images coursed by the switched-capacitor process.


J1B
AUDIO RIGHT
J1A
AUDIO LEFT
PL7
DIGITAL OUT
PL3
CON6
1 2 3 4 5 6
+VM
DGND
-VM
DGND
+5V
D/A CONVERTER / POWER SUPPLY BOARD
132671A
1 2 3 4 5 6 7 8
PL4
I12 S BUS
1 2 3 4
PL2
1 2 3 4 5 6
1510
1511
-VM 18
DGND 17
TTM 16
RAD 15
SIN 14
RE2 13
+VM 12
RE1 11
-5 10
DODS 9
+5 8
TL 7
HF1 6
HFD 5
SI/RD 4
HF GND 3
TRAY 2
DGND 1
1002
1 -VM
2 DGND
3 TTM
4 RAD
5 SIN
6 RE2
7 +VM
8 RE1
9 -5
10 DODS
11 +5
12 TL
13 HF1
14 HFD
15 SI/RD
16 HF GND
17 TRAY
18 DGND
CON18
SERVO/PREAMPLIFIER BOARD
3104 113 3027
SERVO/DECODER BOARD
3104 113 3033


1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
PL4
I12 S BUS
1 2 3 4
PL2
PL3
CON6
1 2 3 4 5 6
+VM
DGND
-VM
DGND
+5V
PL1
CON10
1 +5V
2 +5V
3
4 RSOUT
5 RSIN
6
7 /RESET
8 DGND
9 DGND
10
SUPPLY BOARD
1 2 3 4 5 6
1510
1511
-VM 18
DGND 17
TTM 16
RAD 15
SIN 14
RE2 13
+VM 12
RE1 11
-5 10
DODS 9
+5 8
TL 7
HF1 6
HFD 5
SI/RD 4
HF GND 3
TRAY 2
DGND 1
1002
1 -VM
2 DGND
3 TTM
4 RAD
5 SIN
6 RE2
7 +VM
8 RE1
9 -5
10 DODS
11 +5
12 TL
13 HF1
14 HFD
15 SI/RD
16 HF GND
17 TRAY
18 DGND
CON18
OARD
1701
1 RSIN
2 DGND
3 RSOUT
4 /RESET
1201
SPDIF
1601
I12 S BUS
1 DGND
2 XSYS (XTI)
3 DGND
4 EFAB
5 DGND
6 DAAB (SDATAI)
7 DGND
8 CLAB (BICK)
9 DGND
10 RSAB (LRCK)
11 DGND
12 DEEM
13 ANI
14 ATSB
15 MUSB
16 /MUTE
SERVO/DECODER BOARD
3104 113 3033



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