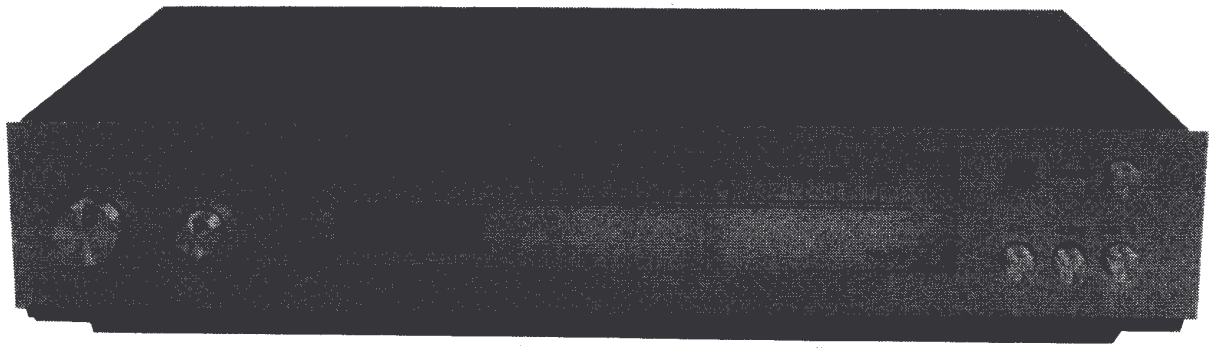
PLL FM TUNER

John Linsley Hood describes an FM tuner using a phase-locked loop demodulator arrangement, to accompany last month's stereo decoder circuit.



I have long felt that the phase locked loop (PLL) is by far the best way of demodulating an FM signal and I have been both surprised and saddened at the way designers of commercial units have neglected this technique. It is especially curious when one sees the lengths to which they go in order to get a little bit lower distortion, or a slightly higher capture ratio — all benefits which are easily obtained with a PLL.

Most contemporary FM tuners use a demodulator circuit of the type shown in Fig. 1. In this the 10.7MHz IF signal is fed from a wide bandwidth amplitude limited amplifier (A1) to a phase detector, (PD1), for which a second input (reference or quadrature) is derived from an ancillary quadrature coil assembly (L2C3).

This quadrature coil circuit is usually driven from a second output point on the limiting amplifier through a small coupling capacitor, C1, or perhaps through an inductor having a similar RF impedance, and is tuned to the mid-point of the 10.7MHz tuning range. The idea is that the phase of the reference input at point A will alter relative to the main signal input as the frequency moves up and down, and will cause the phase detector to give a varying voltage output.

The use of a second, inductively-coupled tuned circuit (L1, C2) added to the quadrature coil helps make the phase/frequency relationship of this circuit more linear, and this improved layout is widely used in the better FM receivers.

There are several snags with this quadrature coil arrangement. The principal one is that the phase of the incoming signal is shifted, as a function of frequency, by non-ideal characteristics in the RF or IF tuned circuits or ceramic filters in the preceding amplifier stages. These phase shifts will cause distortions of the audio output signal because the phase detector cannot distinguish them from actual frequency shifts.

Minimizing these unwanted RF/IF phase shifts is a costly business, which is why tuners with a very low THD figure tend to be very costly.

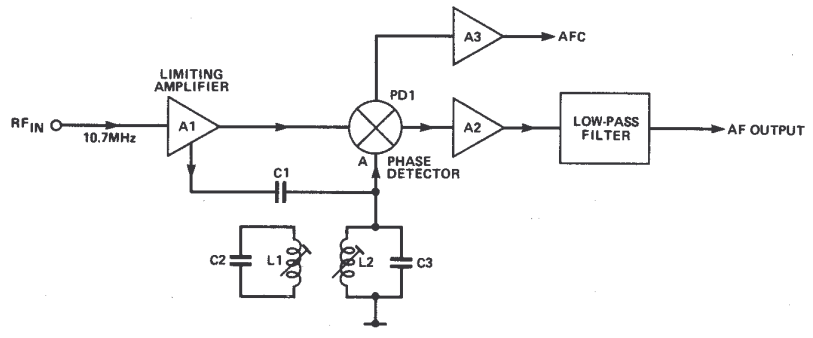


Fig. 1 The quadrature coil demodulator arrangement used in most modern FM receivers.

The PLL Demodulator

This system (shown in Fig. 2) operates by forcing a voltage controlled oscillator to operate in phase and frequency synchronism with the incoming signal — a condition in which the loop is said to be 'in lock'.

If the output frequency of the VCO has a linear relationship with the input control voltage (and with good design this relationship can be very linear indeed) the VCO control voltage will vary with the incoming frequency. The result is an accurate replica of the variations in the incoming frequency — and inadvertent phase errors in the incoming IF signal will largely be ignored.

To make such a system work, the VCO must be tuned so that its natural oscillation frequency (the frequency at which the filtered DC control signal from the phase detector is at its mean potential) is close in frequency to that of the incoming signal. There must also be sufficient gain in the control loop to make it keep in step as the incoming frequency alters.

There will also be a low-pass filter included in the loop to prevent the VCO from chasing its own tail, and it is essential that this

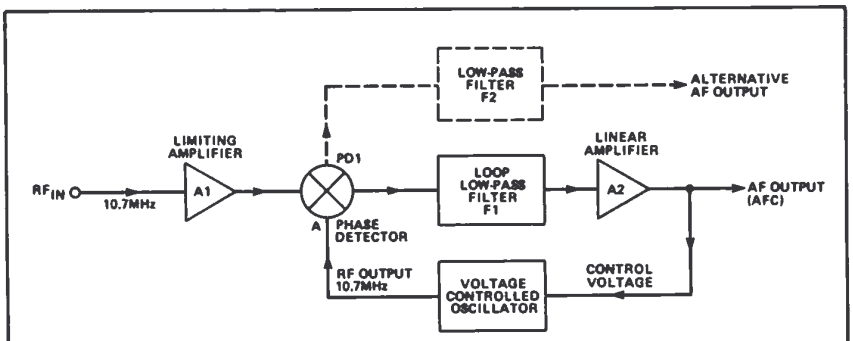


Fig. 2 Basic arrangement of a phase locked loop (PLL) FM demculator.

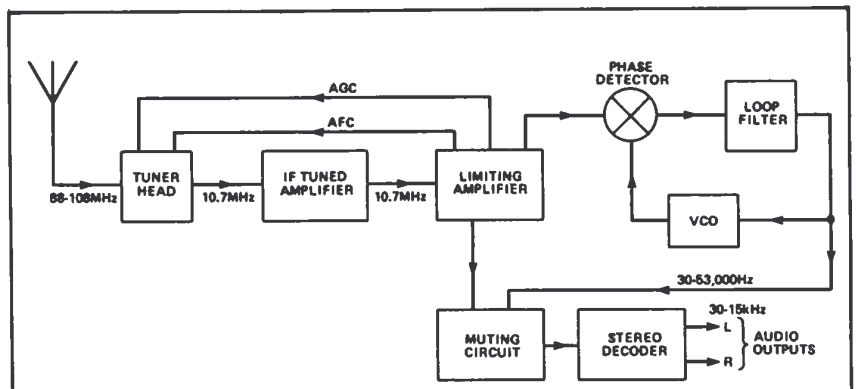


Fig. 3 Block diagram of an FM receiver using a PLL demodulator.

has the correct characteristics to stabilise the loop without restricting its ability to follow fast modulation shifts in the incoming signal frequency. Provided this is done, the control signal fed to the VCO will be an accurate replica of the original signal modulation.

As an alternative, it is possible to take a separate output from the phase detector and give it similar filtration to that of the control loop, thus retaining the quality of the AF signal output but reducing the risk of interfering with the loop operation. This is the layout which I prefer.

Other advantages which the PLL system offers are a very high 'capture ratio' (the ability to reject a slightly weaker interfering signal on the same frequency) and a remarkable ability to extract weak signals from the general background noise. A further useful quality is that the PLL has its own 'selectivity', adjustable by means of the loop gain and quite independent of that of the IF stage. This makes the performance of the receiver(for example, the stereo channel separation) less dependent on the IF stage characteristics, which is useful.

There are, of course, snags — otherwise everybody would use PLLs instead of the technically inferior alternatives. Happily, these snags can be removed by attention to the design and I will refer to this later.

The PLL FM Receiver

Apart from the demodulator stage, the circuit layout of a PLL receiver will be very similar to that of more conventional designs, with a form generally as shown in Fig. 3.

If one of the highly-developed modern FM ICs, such as the RCA CA3189, is used for the limiting IF amplifier and phase detector stages, this can also provide automatic gain control (AGC) and frequency control (AFC) signals to the head amplifier. In addition, since the 3089/3189 ICs are by far the most popular among the commercial circuit designers it is possible that the head amplifier unit will have been designed to suit them which saves a lot of work. The major tasks which then remain are to arrange an adequately linear VCO and to marry this to the 3189.

Two general alternatives exist for a VCO circuit which will operate at the required frequency: an LC tuned circuit system, whose frequency can be adjusted by, say, a varicap diode, or some form of multivibrator. The first of these alternatives gives a pure sinewave output and low noise but it is difficult to get a high degree of linearity since, left to itself, the varicap diode has a highly non-linear capacitance/voltage relationship. This is shown in Fig. 4a.

On the other hand, although it is possible to design multivibrator systems whose operating frequency can be varied by an input control voltage and which have a high degree of linearity in the relationship between output frequency and input control voltage, such circuits usually have the snag that their frequency will drift with changes in temperature. This will spoil the distortion performance of the receiver at the moment of switch-on, before things have settled down. Unfortunately, the problem becomes worse at higher frequencies, and at 10.7MHz it can be a major embarrassment.

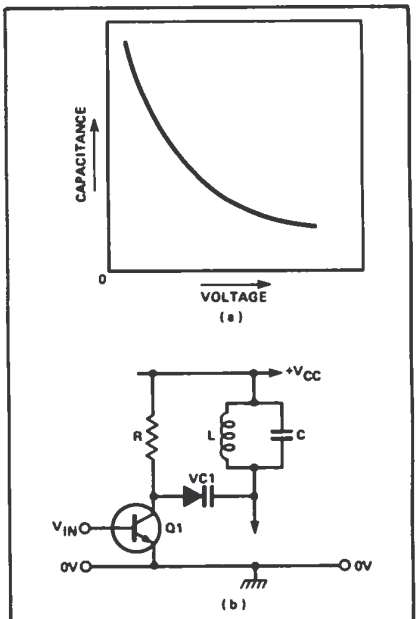


Fig. 4 (a) The capacitance/voltage characteristic of a varicap diode and (b), a circuit in which the non-linear collector current/base voltage characteristic of a silicon transistor is used to balance out the non-linearity in the varicap diode characteristic.

Happily, a technique exists for linearising the voltage/frequency characteristics of a varicap tuned circuit (Fig. 4b). The curvature in the way in which the collector current of a silicon transistor varies as the base voltage is increased is balanced against the varicap diode voltage/frequency non-linearities, and if the correct value of R is used for the transistor and varicap diode chosen the overall linearity can be very good.

A practical VCO circuit layout is shown in Fig. 5 and the excellent linearity of the voltage/frequency relationship is shown in Fig. 6.

In this circuit Q17 is an input emitter follower which provides the necessary low impedance drive to Q18, and a PNP/NPN pair layout is used for Q17/Q18 to cancel the offset of the base-emitter voltages which would otherwise be affected by ambient temperatures.

Q19 is a conventional grounded-base Colpitts oscillator and the HF output signal is taken from the emitter which is a low impedance point. RV4 is used to set the HF output level.

The Need For Signal Muting

If the voltage/frequency relationship of the VCO is a linear one, the control voltage will alter linearly with input frequency as I have shown in Fig. 7. However, beyond certain frequency limits above or below the frequency to which the VCO is tuned, the loop will lose lock. The width of this frequency band is known as the lock or capture range.

This illustrates the basic problem of the PLL when used as an FM demodulator. If a frequency modulated signal, as at A, B or C in Fig. 7, is presented to the PLL while it is at the centre of the lock range (position B) all will be well and the incoming signal will be accurately demodulated. However, if the signal is at positions A or C then, as the signal swings up and down in frequency, the loop will jump into and out of lock with quite large swings in the output signal voltage.

This would be heard as loud and unpleasant rasping noises as the receiver was tuned into and away from a station. I suppose this is the principal difficulty which has militated against the use of the PLL in the collective view of the tuner designers.

The solution is to ensure that the loop capture range is wider than the IF bandwidth so that the signal is pretty small by the time the loop is about to lose lock. A good quality 'muting' system can then be used to disconnect the AF output circuit when the signal strength at the loop input falls below some predetermined value.

With this improvement, the behaviour of the PLL receiver from the listener's point of view is quite impeccable with silence in the gaps between clean, low distortion received signals.

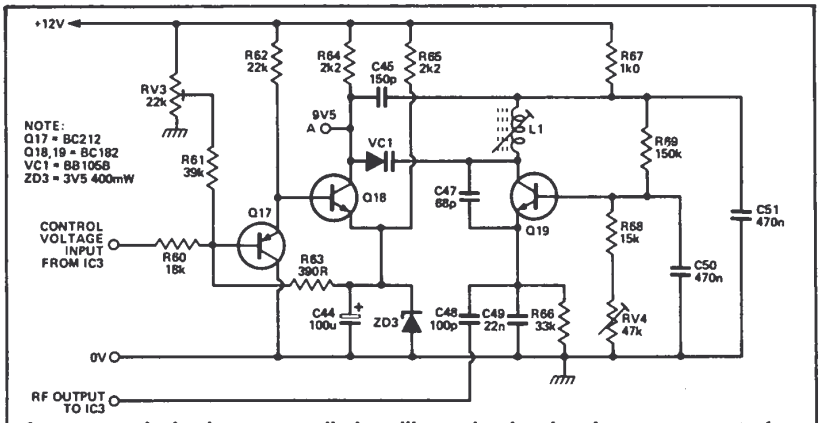


Fig. 5 A practical voltage controlled oscillator circuit using the arrangement of Fig. 4 b to achieve linearity with a varicap diode. Note that the component numbering used here and in Figs. 8, 9, 11 and 12 follows on from the numbering used in last month's stereo decoder circuit.

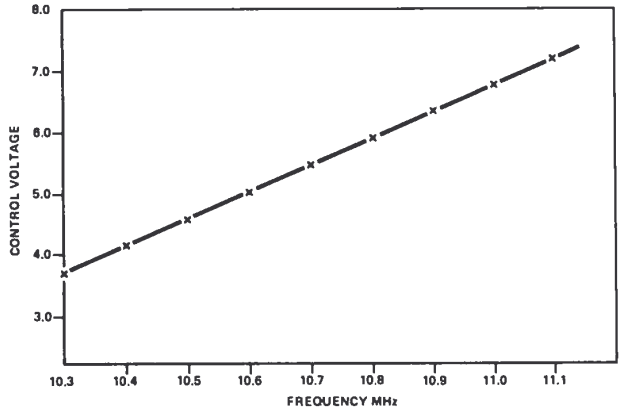


Fig. 6 The control voltage/frequency characteristic of the circuit shown in Fig. 5.

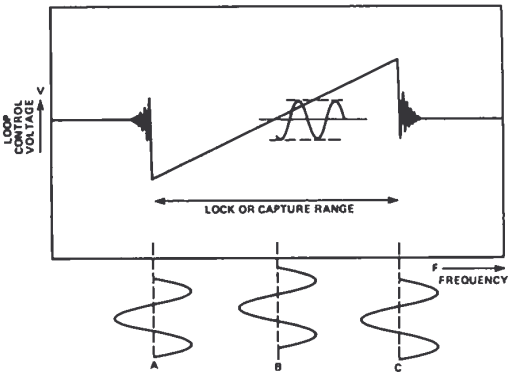


Fig. 7 The control voltage/frequency characteristic is linear only over a certain range and above and below these limits the loop will fail to lock. Signals with a frequency at the limits of the range (A and C) will cause the circuit to swing in and out of lock.

Considering the separate circuit building blocks shown in Fig. 3, I have opted to use a commercially available tuner head unit. There are quite a number of these available, differing in price and specification but all offering a 10.7MHz IF output.

There is no particular reason why this PLL tuner design should not be built using any head unit available to the constructor.

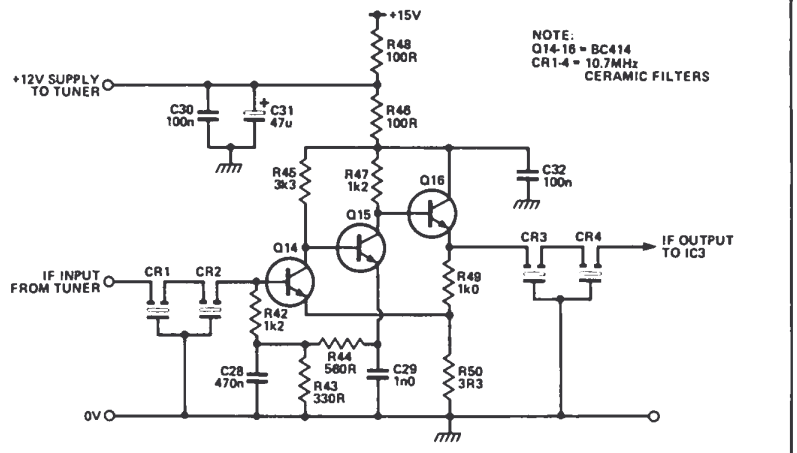


Fig. 8 The 10.7MHz selective IF amplifier circuit.

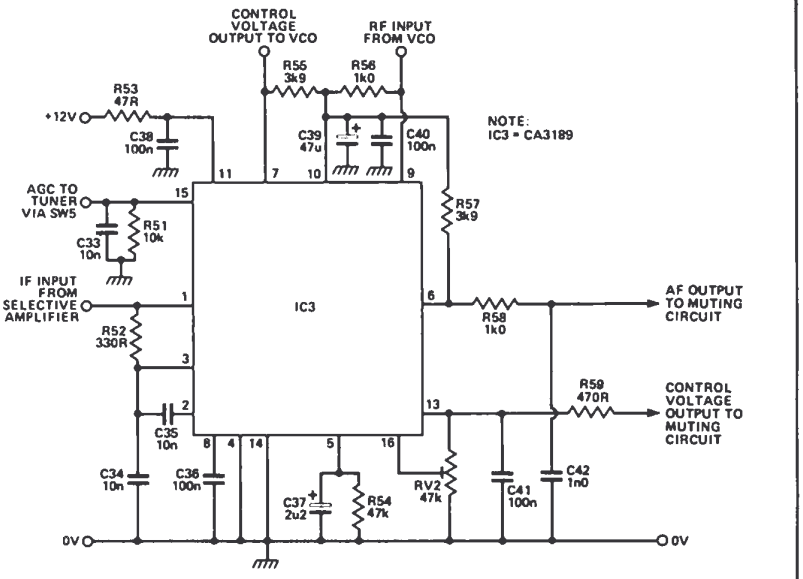


Fig. 9 The circuitry around the CA3189.

However, for the prototype I chose the ALPS FF317U which is a well-designed and sensitive unit, readily available at a reasonable price. This is a variable capacitor tuned unit, avoiding the need to apply thermal compensation to the tuning voltages which would be needed in a varicap tuned unit.

It also has the practical advantage that it is designed to work in harness with the 3189 demodulator IC, so both the AGC and AFC voltages from the IC are suitable for this tuner head. Additionally, as is becoming a fairly common feature with such tuner heads, the IF output impedance is 300 ohms which means it can be directly connected to the input ceramic filter of the tuned IF amplifier.

In order to exploit the high sensitivity of the PLL, which is helped by the characteristics of the 3189, I have used a high gain, three transistor IF amplifier using two pairs of cascaded 10.7MHZ ceramic filters. The complete IF amplifier circuit is shown in Fig. 8 and is based on a wide bandwidth, gain stabilised layout derived from the old valve-type 'ring of three' circuit which has excellent characteristics. Moreover, the performance is not particularly affected by the transistor types used so although I have specified BC414s as a good, modern, low noise type, BC184s would work just as well.

The ceramic 'ladder filters' are a convenient and compact way of obtaining selectivity but they have the disadvantage that they introduce a substantial degree of attenuation from input to output when compared with a tuned circuit. Typically, a single filter element will lead to a signal loss of 3x. Two, in series, will increase this insertion loss to 5x. If, therefore, two pairs are used, the total signal loss through the filters will be 25x.

The design value for the overall stage gain of the 10.7MHz amplifier of Fig. 8 is 14x, so the stage gain from Q14 to Q16 needs to be 350x. This is set by the feedback resistors R49 and R50. All of the resistors should be reasonably non-inductive, which rules out a wire-wound component for R50.

The tuner head IF output impedance is 300 ohms and since this is the required input/output impedance for the ceramic filters the IF output from the tuner head can be taken directly to CR1.

The circuit connections to the CA 3189 (Fig. 9) are much as recommended by the makers, except where circuit modifications are needed to make it operate within a PLL. There is not space here to discuss in detail the internal circuitry of the 3189, which is an ingenious and carefully designed component. However, in simple terms the input to the limiting amplifier is at pin 1 and the DC bias for this is taken from pin 3. An AGC signal is available from pin 15, which sits at about +6V until the input signal exceeds a value determined by the setting of RV2.

Two audio output points are provided. One is taken from pin 6 and can be controlled by an internal deviation muting circuit, while the other is taken from pin 7 and cannot. I have chosen to use the pin 6 output for the audio signal and that from pin 7 (normally used to operate a centre zero tuning meter and AGC circuitry) as the control voltage output to the PLL.

Since I am using a high quality external muting circuit, I have disabled the muting level control for which pin 5 is provided.

The Muting Circuit

As I mentioned earlier, the ability to use a phase locked loop system to demodulate an incoming FM signal (as distinct from the ubiquitous PLL circuit used in the stereo decoder) depends entirely on the designer's ability to suppress the nasty noises which would otherwise occur on tuning the receiver into and away from a station.

The method I have used for this

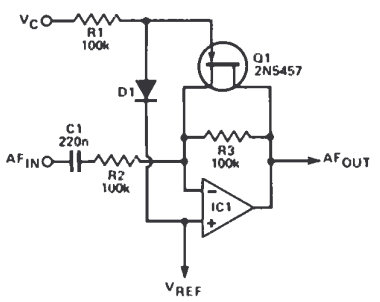


Fig. 10 A simple FET muting circuit.

Oscillogram showing a linear change of voltage at the audio output of the receiver as an RF input signal is swept in frequency from 95.2 - 95.6MHz. The horizontal scale represents 10kHz/ division and the vertical scale is set at 300mV/ division.

is shown in simplified form in Fig. 10. A good quality, low distortion op-amp (such as an LF351/3 or a TL071/2 is connected as a unity gain inverting amplifier. I am satisfied that even the most critical audiophile will not fault such an op-amp in unity gain mode. A junction FET (Q1) is then connected across the feedback resistor. When this is conducting the gain of the stage is very nearly zero and any distortion due to the non-linearity of the FET is irrelevant.

If the FET is biased off it becomes an extremely high impedance indeed and, again, there is no significant effect due to its connection across R3. The diode D1 is included to prevent the FET gate from being biased into conduction, which would disturb the DC output level from the op-amp.

This circuit is incorporated, in practical form, in the muting stage shown in Fig. 11. In this, the output voltage for the signal strength meter from pin 13 of the 3189 (which varies from about 0.8V to between 3 and 4V) is taken to one half of a dual op-amp which converts it to a +14 to +1V swing from noise threshold to signal levels.

Since the TL071/72 does not include 0V as a permissible input level when run from a single supply line, Q20, D1 and R72 are used as a DC level shifting network. The preset (RV5) is used to set the level at which IC4a output swings from +14 to +1V, to convert the FET (Q21) from its short circuit to its open circuit condition.

The muting circuit can be disabled by SW3, which biases the FET (Q21) into an open circuit state under all signal conditions. The audio output from the tuner is taken from the output of IC4b to the stereo decoder circuit described last month.

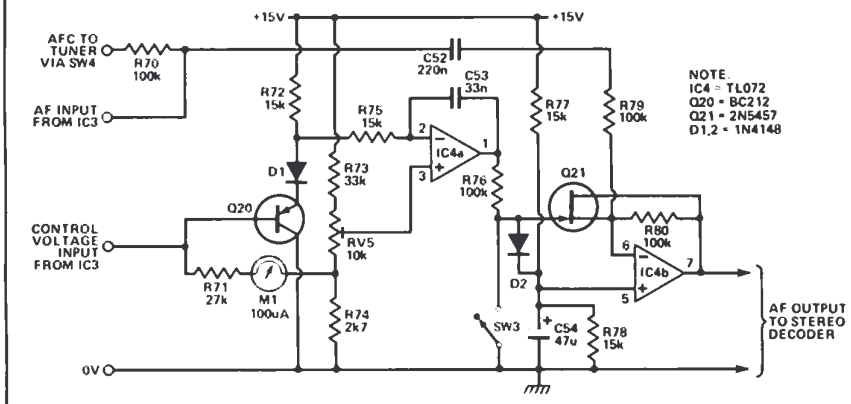


Fig. 11 A practical muting circuit incorporating the FET arrangement of Fig. 9.

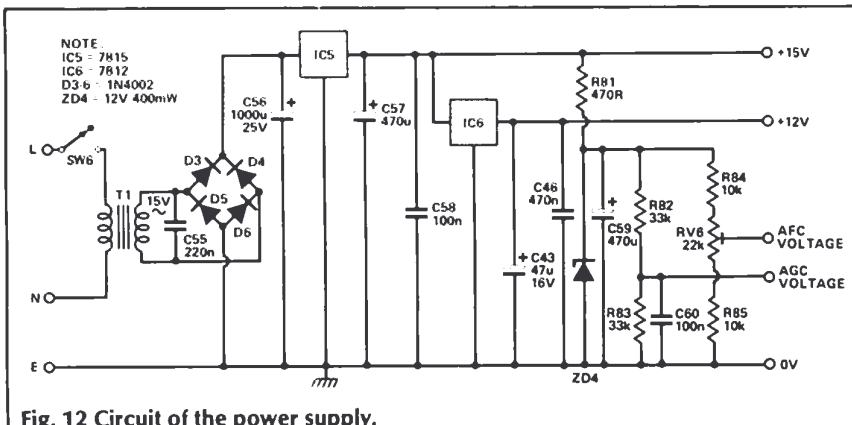


Fig. 12 Circuit of the power supply.

AFC And AGC Connections

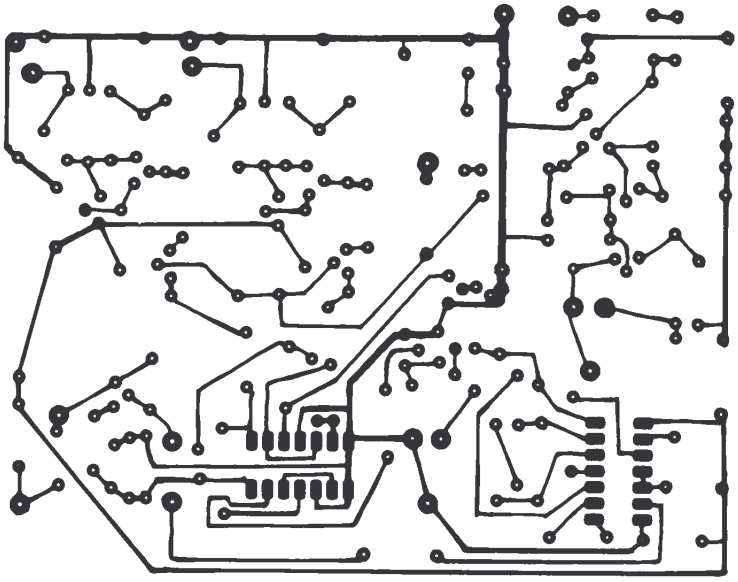
The output voltage at pin 6 of the 3189 normally sits at about 5–6V under no signal conditions and will swing up and down by about ±1V on tuning through a signal. This can be used as an AFC signal to the head but there should be no shift of tuned position when the AFC is switched in. This is achieved by using RV6 (Fig. 12). To preset the same voltage level as that from the 3189.

The AGC control voltage level, taken from pin 15 of the 3189, will normally sit at about 6–8V on no signal. An equivalent potential is set by R43 and R44 for the AGC off setting. The whole tuner circuit is powered by a single +15V supply, but because the VCO is voltage operated, it is essential that the positive line supply voltage to this is held constant. This is done by inserting a standard 12V IC voltage regulator, IC6, between the input +15V supply and the 12V line which feeds the CA3189 and the VCO.

This project will be concluded with a description of the construction and setting up of the complete FM tuner.

ETI

PCB FOIL PATTERNS



The foil pattern for the Stereo Decoder Board, held over from last month.