

Dolby Laboratories Inc Information

TECHNICAL DATA FOR PRIVATE CONSTRUCTORS

Introduction

This information is provided to enable the private constructor to build Dolby B-type processors which are switchable between encode and decode functions. It is envisaged that such processors will be used as separate units to add on to existing cassette or open-reel recorders, FM tuners and receivers, or incorporated as integral parts of new equipment under construction. The processors will enable Dolbyized tapes to be recorded on the user's own equipment, and will reduce the high frequency noise level of these tapes and also that of Dolby encoded FM broadcasts and pre-recorded tapes by 10 dB.

Contents

The information provided for private constructors consists of:

1. Obligations relating to use.
2. Construction of the Dolby B-type circuit.
3. Alignment procedure
4. Check of characteristics.
5. Application of the circuit to an open-reel or cassette recorder.
6. Circuit operation
7. Circuit diagram, response curves and reference data.

1. Obligations relating to use

This information is provided for private use only. Those using it are required to accept the following restrictions:

- 1.1. The technical information and schematic diagrams may not be copied or used for any commercial purpose.
- 1.2. The provision of the information contained herein does not constitute a license either explicit or implied to manufacture Dolby B-type noise reduction processors for sale, lease or any commercial benefit.



Dolby and the double-D symbol are trade marks of Dolby Laboratories Inc.

731 Sansome Street
San Francisco CA 94111
Telephone (415) 392-0300
Telex 34409

346 Clapham Road
London SW9 9AP
Telephone 01-720 1111
Telex 919109

2. Construction of the Dolby B-type Circuit

2.1 Construction

The circuit is most conveniently constructed on "Veroboard" or "Lektrokit". Alternatively, a printed circuit layout may be purpose-designed. As individual requirements differ so widely, printed circuit layouts and printed circuit boards are not available from Dolby Laboratories.

2.2 Component Tolerances

The values and tolerances specified in the circuit diagram must be adhered to exactly in order to ensure matching of the processor's characteristics to the standard Dolby characteristics. Specially selected Fets of the 2N5458 family must be used; suitable devices are available from Dolby Laboratories, price 50p (\$1.25) each.

2.3 Circuit Configuration

The processor shown in the circuit diagram is of the switchable type, intended to provide the basic Dolby functions for a tape recorder with minimum circuit complexity. The circuit may be wired permanently in either of its two modes if required. Possible instances are the use of the processor in decode mode in an FM tuner, and the use of two processors per channel, one in encode, the other in decode, in 3-head recorders where off-tape monitoring in the decoded form is required. Those using switchable processors in conjunction with a tape recorder will make operation on the units more convenient if they link the mode switching of the processors with that of the recorder, e.g. by using a relay.

2.4 Power Supply

Although the circuit diagram specifies a 12V supply, voltages between 12 and 24V may be used without circuit modification. Component values are optimized for 12V, however, so increasing the rail voltage will not substantially increase the maximum output level before clipping beyond the 12 dB above Dolby Level of the 12V circuit. Each processor draws about 20mA from a 12V supply. Supply ripple should be less than 300 μ V.

3. Processor Alignment

- 3.1 After construction, the GAIN and LAW presets must be adjusted to give the correct noise reduction characteristics. This should be carried out with the processor connected to a power supply having an output voltage equal to that on which the unit will eventually run.

3.2 Equipment Required:

Oscillator

A. C. Millivoltmeter

3.3 Alignment Procedure

3.3.01 Switch NOISE REDUCTION (NR) and MPX filter off

3.3.02 Short Fet gate to ground

3.3.03 Adjust LAW control for maximum voltage on Fet source

3.3.04 Set oscillator frequency to 5.0 kHz and its output voltage to about 1 mV

Connect oscillator to processor input

Decode only processors: proceed to section 3.3.12

Encode only and switchable processors: continue

3.3.05 Switch switchable unit to encode

3.3.06 Connect millivoltmeter set to 30 mV range to processor Monitor Point

3.3.07 Adjust oscillator output until meter reads 17.5 ± 0.1 mV

3.3.08 Transfer meter to Record Amp Point: meter should read $17.5 \text{ mV} \pm 1 \text{ dB}$

Note the meter reading in dB. Switch on NR

Adjust GAIN control until meter reading increases by 10.0 ± 0.25 dB

3.3.09 Remove Fet gate short. Adjust LAW control until meter reading falls by 2.0 ± 0.25 dB

3.3.10 Re-apply Fet gate short. Check that meter reading rises to exactly the level set in 3.3.08 above

Encode only processors: proceed to section 3.3.17.

Switchable processors continue:

3.3.11 Switch unit to decode and NR off. Ensure Fet gate short is on

3.3.12 Connect meter set to 100 mV range to Monitor Point. Adjust oscillator output level until meter reads 44.0 ± 0.1 mV.

Note meter reading in dB

3.3.13 Switch NR on. Check that meter reading falls by 10.0 ± 0.5 dB

Switchable processors: proceed to section 3.3.17

3.3.14 Adjust GAIN control until meter reads 10.0 ± 0.25 dB below that noted in section 3.3.12

3.3.15 Remove Fet gate short. Adjust LAW control until meter reading rises by 2.0 ± 0.25 dB

3.3.16 Re-apply Fet gate short. Check that meter reading falls to exactly level set in 3.3.14 above

- 3.3.17 The GAIN and LAW adjustments should then be locked to prevent the settings being disturbed. They will not require adjustment unless any of the components or the power supply voltage are changed.
- 3.3.18 Switch NR off. Increase oscillator output until meter reads 580 mV. Increase oscillator frequency to 19.00 kHz. Switch in MPX filter and adjust inductor L2 for minimum reading on meter (should be at least 30 dB below 580 mV).

4. Characteristics Check

After completing the alignment procedure, it is necessary to check that the processors have the correct transfer characteristics. The following characteristics check procedure relevant to the type of processor under test should be followed:

4.1 MPX Filters

Processors with switchable MPX filters should be tested with their filters switched out. Those with permanent filters should be tested as described, but the test limits only hold as far as 15 kHz.

4.2 Encode only processors and switchable processors in encode:

4.2.01 Switch NR off. Connect meter to Monitor Point of processor.

Adjust oscillator frequency to 400 Hz.

Adjust oscillator output level until meter reads 29 ± 1 mV.

4.2.02 Transfer meter to To Record Amp. Point. Switch NR on.

4.2.03 Check that meter reading varies with frequency within ± 1 dB of the -26 dB curve of figure 1 up to 10 kHz and ± 1.5 dB beyond.

4.3 Decode only processors and switchable processors in decode.

4.3.01 Switch NR on. Connect meter to Monitor Point of processor

4.3.02 Adjust oscillator frequency to 140 Hz and output amplitude until meter reads 29 ± 1 mV.

4.3.03 Adjust oscillator output amplitude with frequency according to the -26 dB curve of figure 1 and check that the level at the processor Monitor Point remains at 29 mV ± 1 dB up to 10 kHz and ± 1.5 dB beyond.

4.4 Encode and decode processors which are intended to be used together as pairs can be checked for compatibility of characteristics as follows:

4.4.01 Connect the Record Output of encode processor to ground via a 10 k resistor in series with a 1k potentiometer. Connect wiper of potentiometer to the input of decode processor.

- 4.4.02 Switch NR off. Connect oscillator to input of encode processor, adjust its frequency to 400 Hz and amplitude until the meter connected to Monitor Point of encode processor reads 29 ± 1 mV.
- 4.4.03 Transfer meter to the Monitor Point of decode processor and adjust the 1k potentiometer until meter reads 29 ± 1 mV.
- 4.4.04 Switch NR on. Sweep frequency of oscillator and check that meter continues to read $29 \text{ mV} \pm 2 \text{ dB}$.

5. Application of the Circuit to a Tape or Cassette Recorder

5.1 Suitability of Dolby B noise reduction.

The Dolby B-system is designed to reduce noise in consumer recording or transmission media. In the case of tape, encompassing the range from 19 cm/s half track on 6.25 mm tape down to 4.75 cm/s quarter track on 3.81 mm tape, high frequency noise, i. e. hiss, is the major source of noise. The Dolby B characteristic is also effective in other media in which the predominant noise is hiss, such as FM stereo broadcasts.

It should not be used where there is a wide-band noise spectrum, as with 38 cm/s tape and optical soundtrack. Removing the high frequency noise in these cases only serves to emphasize the remaining mid- and low-frequency noise. In these applications, the Dolby A-system, which gives 10 dB of noise reduction across most of the audio spectrum, rising to 15 dB beyond 10 kHz, should be used.

5.2 Incorporation of Processors into the Record/Replay Chain

Whether the processors are used in a separate add-on unit or permanently installed, they should be connected into the record/replay chain as shown in the block diagrams.

5.3 Tape Recorder Characteristics

The gain of the tape recorder, measured between the Meter Point of the processor in record and replay must be unity and the frequency response flat to ensure fully complementary characteristics. Optimum results will not be obtained if the frequency response of the recorder does not extend at least to 10 kHz, unless a similar restriction is placed on the bandwidth of the input signal before the record processor.

5.4 Dolby Level and Calibration

The standard Dolby characteristics are related to specific flux levels on the tape to ensure compatibility between all Dolby-equipped hardware and all Dolbyized software. To obtain this relationship the voltage at the Meter Point of the processor must be 580 mV when playing or recording the reference flux. This is achieved by adjusting the play calibration potentiometers located at the input of the processors in replay and the record calibration potentiometers located at the output of the processors in record. The following procedure should be used:

- 5.4.01 The recorder should be fully checked out to optimise response, set bias, minimize hum, etc.
- 5.4.02 Connect millivoltmeter to Meter Point. Switch NR off. Set processor to PLAY.
- 5.4.03 Play level set tape recorder to Ampex operating level (185 nWb/m) for reel-to-reel or to 200 nWb/m for cassettes. Adjust PLAY CAL for 580 mV on meter.
- 5.4.04 Connect oscillator to processor input. Put on the recorder a reel of tape for which it is correctly biased. Set recorder and processor to RECORD. Feed in a 400 Hz signal from the oscillator. Adjust oscillator output and record level until meter reads 580 mV.
- 5.4.05 Record a section of tape, rewind, replay and check meter reading. It should be $580 \text{ mV} \pm 1 \text{ dB}$. If it is not, adjust the REC CAL control in the appropriate direction and repeat the record and replay process until it reads 580 mV.

If separate record and replay processors are used on a three-head machine, the sequential record-replay procedure is not necessary; the record calibration may be performed as follows:

- 5.4.06 Repeat section 5.4.04 above. Transfer meter to Meter Point of replay processor.
- 5.4.07 Adjust REC CAL until meter reads 580 mV.

5.5 Notes on calibration

PLAY CAL will not normally need resetting, but should be checked occasionally, especially in cases where the noise reduction unit is in the form of an add-on unit.

REC CAL must be adjusted every time a different brand or type of tape is used. It is wise to check it regularly, especially in the case of add-on units, and before important recordings are made.

It should be noted that the reference flux level is simply for reference, and is in no way to be regarded as a recommended maximum record level. It is worth noting that when using the Dolby noise reduction system there is the option of recording at a lower level than normal, exchanging some of the 10 dB of noise reduction for a reduction of distortion at peak record level.

5.6 Adjustment of Record and Replay levels during normal operation

Once calibrated, a fixed relationship exists between the output of the head preamplifier and the processor in replay and between the recording amplifier and the processor in record. This means that user-operable output level controls must be located after the output of the processor in replay, and that record level controls must be located in front of the input of the processor in record. This presents no problem if the processors are being incorporated as part of a new design recorder.

If the processors are used as add-on units, record level and output level controls must be provided in the correct location as part of the add-on unit.

5.7 Preservation of Calibration When Using Add-on Units

When an add-on unit is being used with a tape recorder, and is connected to the tape recorder's normal input and output points, the recorder's own input and output controls form part of the record and replay calibration chains respectively. Once set during calibration, they must not be touched again, otherwise the calibration will be destroyed. It is wise to mark the settings of these controls so that if they are accidentally displaced, this can easily be noticed. Setting of record and output levels is done in the normal manner, but the appropriate controls on the noise reduction unit are used.

5.8 Evaluation of Performance of Noise Reduction Unit in Conjunction with Tape Recorder.

5.8.01 Frequency Response Measurement

After calibration, it is worthwhile checking the overall frequency response of the recorder with the noise reduction switched off, and then with it switched on. This is best done at about 26 dB below Dolby Level, and the addition of noise reduction should not more than double any deviation from flat response present without noise reduction. If there are greater deviations than this, recheck the record calibration. If this is correct, it is likely that the processor characteristics are being upset by the presence of residual bias signals. This can be confirmed by repeating the processor characteristics check detailed in 4.2 above with the bias oscillator running. The difference between characteristics with the oscillator on and off should be less than 1 dB. On systems with record and replay processors, the replay processors should also be checked. If bias is found to be the cause of the trouble, attention should be paid to correct tuning of such bias traps as there are within the machine, and to screening the processors from picking up radiated bias signals. Note that the addition of a parallel LC circuit, resonant at bias frequency, between the emitter of Q104 and the resistor and capacitor normally attached to it will usually help in this situation.

5.8.02 Noise Measurement

The Dolby B circuit gives 10 dB of noise reduction at 5 kHz and above. The measured signal-to-noise ratio depends on the noise spectrum of the equipment being measured and the weighting network (if any) being used. Unless hum components are kept very low, unweighted signal-to-noise comparisons between 'noise reduction on' and 'noise reduction off' conditions yield disappointing numerical results and undervalue the audible

effect of the noise reduction. A closer numerical approximation to the audible effect is obtained if a DIN, IEC or NAB weighting filter is used. With the DIN filter, over 9 dB signal-to-noise ratio improvement should be possible using cassettes, and over 8 dB for 9.5 cm/s quarter track open reel.

5.8.03 Input Signal Requirements

The Dolby system will only reduce noise generated after the record processor and before the replay processor. If the input signal is noisy, or passes through a noisy stage before the record processor, the noise present with the input signal will be reproduced at the output of the replay processor with the same high fidelity as the input signal itself.

6. Circuit Operation

6.1 Input Stage

The input stage is fed to transistor Q1, providing gain and correct source impedance for the low pass filter, which attenuates all unwanted frequencies (such as tape recorder bias or FM multiplex signals) to a level of less than -45 VU. If such spurious signals are above the threshold of the compressor, the full 10 dB of low-level pre-emphasis will not be obtained.

The 19 kHz notch filter (L2 and C2) may be switched out if a response up to 20 kHz is required. This should not be done if the signal source is an FM tuner, however, not only is it pointless, due to the limited frequency response of the source, but there are few tuners whose output of multiplex components is below -45 VU. The L2 C2 section of the filter may be omitted from replay-only processors in recorders but must, of course, be included in decode-only processors used in FM tuners and receivers.

6.2 Second Stage and Mixing Amplifier

Transistors Q2/Q3 provides gain and also have a low output impedance to drive the dynamic filter and monitor output in the encode mode. This stage also has a high output current capability to drive the simple meter circuit on the circuit diagram. At this point, the signal splits into two paths, one via resistor R14 to the inverting mixing amplifier comprising transistors Q4/Q5, and one via the dynamic filter to the side-chain. The output of the side chain is then added to the main signal in the mixing stage and thus modifies the amplitude of the main signal at low levels and high frequencies.

6.3 The Dynamic Filter

The dynamic filter consists of capacitors C6, C7, C101, resistors R101, R102 and the source-drain resistance of Fet Q101. C6 and C7 form a capacitive divider which reduces the amplitude of the signal at

the input of the dynamic filter from 580 mV to 100 mV. This arrangement allows the stages driving the filter to operate at the 580 mV level, which is high enough to be regarded as a suitable output voltage without the need for further amplification (and hence an output stage) and allows the dynamic filter to operate at 100 mV at which level the second harmonic distortion produced by the Fet remains low without the addition of distortion cancellation circuitry.

6.4 Noise Reduction Amplifier

At low levels, the Fet is biased off, and thus has a high source-drain resistance; the response of the side chain is then controlled by capacitors C6 and C7 in parallel and resistor R101. The output of the filter is amplified by the transistors Q102/Q103 and fed via the attenuator consisting of the resistors R110 and R113 and the mixing resistor R15, to the mixing amplifier where it is added to the main signal. The output of the mixing amplifier forms the record output of the processor. The low level gain of the side chain is such that the record output is increased by 10 dB at 5 kHz when the side chain signal is added to the main signal. Figure 2 shows the low level response of the record output.

6.5 The Integrator

The side chain output is further amplified by transistor Q104, rectified and then smoothed by the non-linear integrator consisting of resistors R120 and R121, capacitors C109 and C110, and diode D105. The D. C. output of the integrator is fed to the gate of the Fet via resistor R122 and controls the source-drain resistance of the Fet.

6.6 Control Mode

When the D. C. control voltage becomes sufficient to overcome the off bias set on the source of the Fet by the Law control, RV 101, it causes the resistance of the Fet to decrease. This causes the turnover frequency of the second half of the filter to increase attenuating low and medium frequency signals in the side chain. With increasing input levels, therefore, the contribution of the side chain signal to the combined record output signal is reduced, producing the transfer characteristics plotted in figure 2. At 0 VU, the side chain signal is so small compared with the main signal that its effect can be ignored. The control circuit utilizes a two-stage non-linear smoothing scheme to avoid the generation of modulation products while providing fast response under transient conditions. For small changes in signal level the diode D105 is non-conductive, the time-constant R121 and C110 then providing a high degree of smoothing. However, for sudden increases in signal level the diode conducts and quickly reduces the gain of the circuit.

6.7 Overshoot Prevention

Clipping diodes D102/D103 prevent transient overshoots. Normally, the signal level across the diodes is such that they are non-conducting, but under extreme transient conditions when the side chain is re-establishing its operating point, these diodes limit the side chain signal output. Thus for a short period of time, the record output consists of a large pure signal (from the main path) mixed with a small amplitude clipped component (from the side chain). Because of the small amplitude of the side chain addition to the main path signal the overall distortion is small and, as it lasts for a short period of time, just after a transient, is inaudible. The maximum overshoot amplitude is less than 2 dB.

6.8 Distortion Reduction

To reduce the amount of second harmonic distortion produced by the Fet an a. c. signal equal to half the amplitude of the signal appearing on the drain and in phase with it is superimposed on the D. C. control signal on the gate. This signal is derived from the potential divider R117/R124 located in the emitter of transistor Q104.

6.9 Action of circuit in decoder mode

In the decode mode, the same circuitry is used, but the functional blocks are rearranged so that the side chain forms a negative feedback loop around the mixing amplifier. The decode characteristics are therefore complementary to the encode characteristics enabling an overall flat frequency response to be attained. At 0VU, therefore, where the side chain signal is small, the decode gain of the processor is normal, but as the level is reduced the significance of the side chain signal increases and the gain of the processor is reduced by up to 10 dB at high frequencies.

7. Circuit Diagram, Response Curves and Reference Data

7.1 Reel-to-reel level set tapes may be obtained from:

Angus McKenzie Facilities Ltd.
57 Fitzalan Road
London N3

7.2 Level set cassettes may be obtained from:

Metrosound Manufacturing Co.
Audio Works
Cartersfield Road
Waltham Abbey
Essex

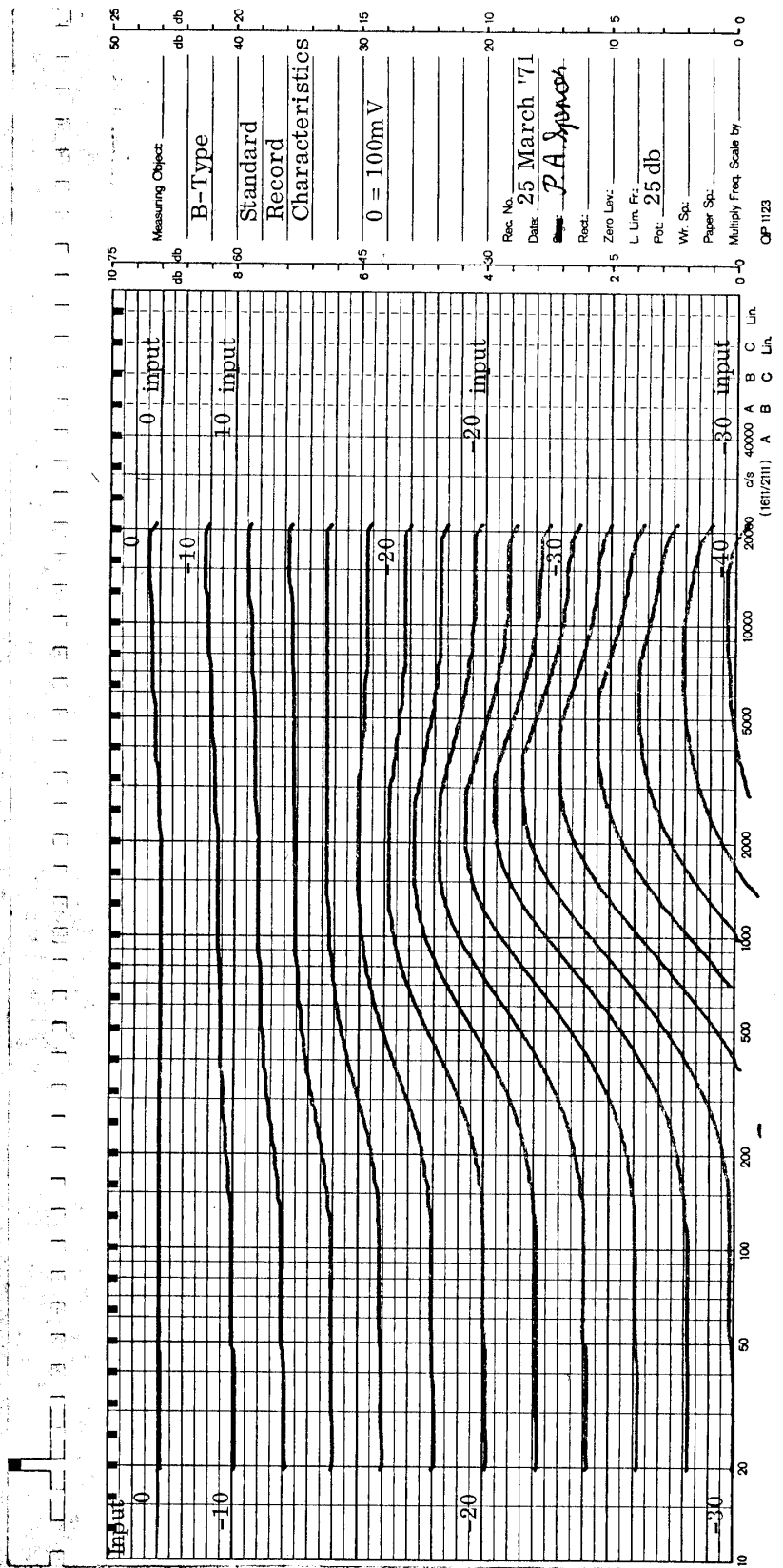
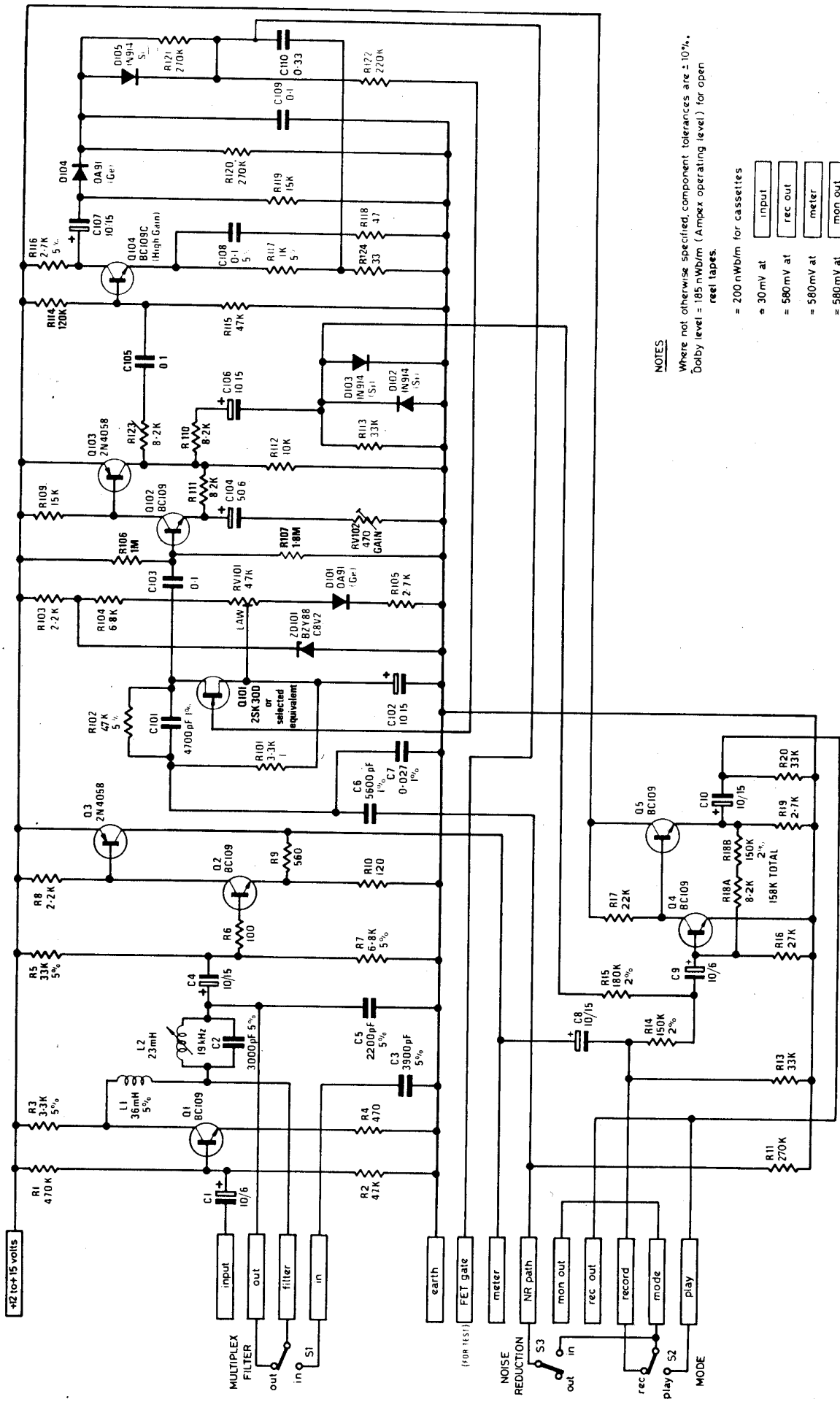


Fig. 1. Record Processor Characteristics



NOTES
 Where not otherwise specified, component tolerances are $\pm 10\%$.
 Dolby level = 185 nWb/m (Ampex operating level) for open reel tapes.

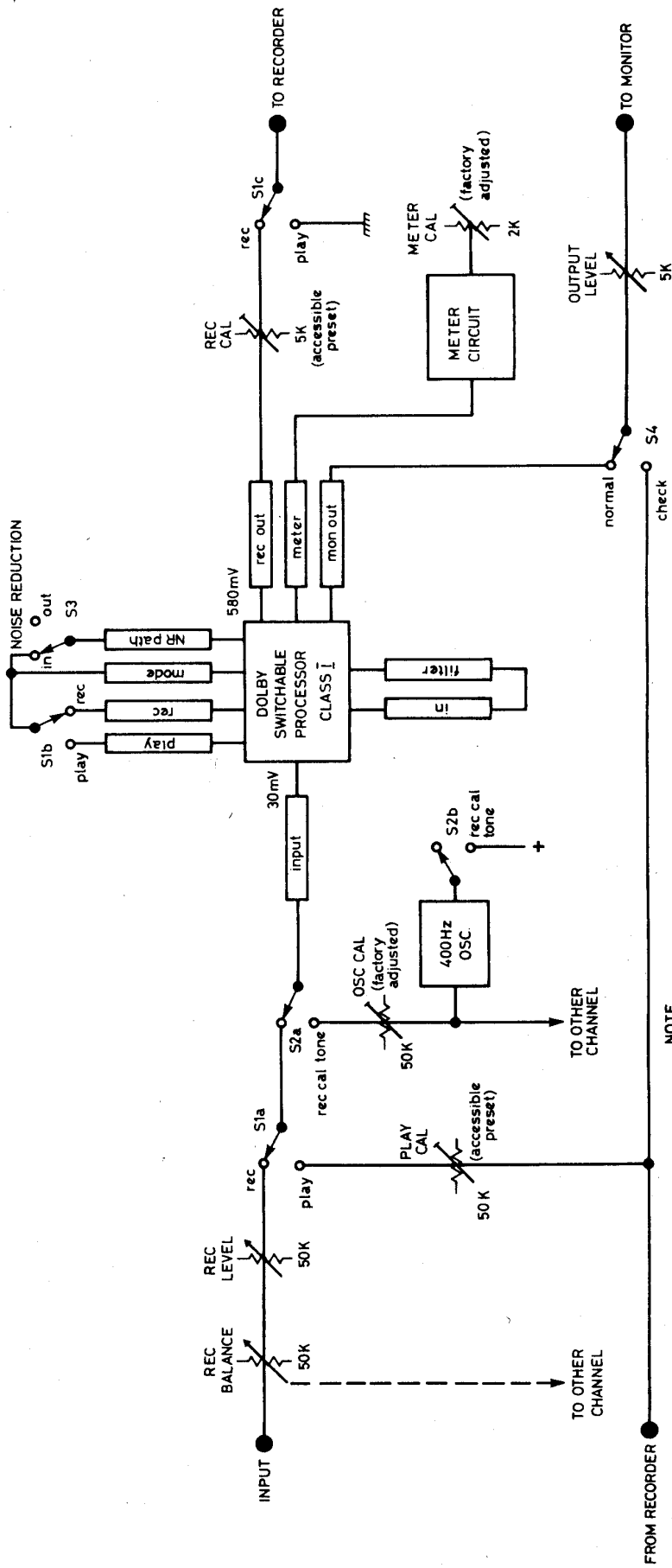
- = 200 nWb/m for cassettes
- = 30 mV at input
- = 580 mV at rec out
- = 580 mV at meter
- = 580 mV at mon out

CLASS I

DOLBY LABORATORIES INC

Proprietary information for Licensing and Evaluation Purposes only. The information given herein may not be used commercially without the prior written agreement of Dolby Laboratories Inc.

DISCRETE COMPONENT SWITCHABLE PROCESSOR WITH MULTIPLEX FILTER
 CLASS I Drawing No. AIC 845 © Dolby Laboratories Inc 1972



NOTE
 1. Processor to include multiplex filter

B-TYPE NOISE REDUCTION UNIT, SWITCHABLE
 Drawing No A2B 785 © Dolby Laboratories Inc. 1972

DL DOLBY LABORATORIES INC
 Proprietary information for Licensing and Evaluation Purposes
 only. The information given herein may not be used commercially
 without the prior written agreement of Dolby Laboratories Inc