SECTION II

RMS-DC CONVERSION – BASIC DESIGN CONSIDERATIONS

ACCURACY OF RMS-DC CONVERTERS

An ideal rms converter would provide a "dc" output voltage exactly equal to the rms value of its input voltage, regardless of the amplitude, frequency, or wave shape of the input waveform. Of course a practical rms converter does have some errors. In the following sections, we will discuss these errors and their overall effect on rms converter performance.

First, we will discuss the low frequency or "static" errors. Next, we will review the effects of bandwidth on accuracy. Then, we will present in some detail the effect of the converter's averaging time constant. Finally, we will discuss the effect of wave shape, e.g., pulses, noise, SCR controlled sinewaves, on the rms converter's accuracy.

"Static" Errors – rms-dc Converter Static Errors and Their Effect on Overall Accuracy

Static errors are those offsets and scale factor errors which apply to "dc" or moderate frequency ($\simeq$1kHz) sinewave input signals. Under these conditions, the finite bandwidth of the converter (and the effective averaging time) can be made negligible compared to the input and output offset, and scale factor errors. RMS can be interpreted here as the square root of the low pass filtered (or averaged) square of the input signal voltage.

An rms to dc converter's overall "static" error is specified in percent of reading plus a constant. As shown by Table 2, the AD637J is specified at 1.0mV ±0.5% of reading. This should be interpreted to mean that *at any* point within the AD637J's 0V to 7V rms input dynamic range, the converter's output voltage will differ (at most) from the precise value of the rms input by 1mV *plus* 0.5% of the *correct rms level*. Note that this is less absolute error than the AD536AJ rms converter. To illustrate this point, consider a sinewave input of 1.00V rms at 1kHz applied to the input of an AD637J. The actual AD637 output voltage will be within: ±(1.0mV + 0.5% ×

	AD536AJ	AD637J	AD636J
Input Dynamic Range	7V rms	7V rms	1V rms
Nominal Full Scale	2V rms	2V rms	200mV rms
Peak Trans. Input	±20V	±15V	±2.8V
Max Total Error			
No External Trim	5mV ±0.5% RDG	1mV ±0.5% RDG	0.5mV ±1% RDG
Bandwidth, (−3dB)			
Full Scale	2MHz	8MHz	1.3MHz
0.1V rms	300kHz	600kHz	800kHz
Error at Crest			
Factor of 5	−0.3% @ 1V rms	±0.15% @ 1V rms	−0.5% @ 200mV rms
Power Supply			
Volts	±3 to ±18 max	±3 to ±18 max	+2, −2.5, ±12 max
Current	1mA; 2mA max	2mA; 3mA max	800μA; 1mA max

Table 2. Condensed rms Converter Specifications Table

1.0V) = ±(1mV + 5mV). This equals 6mV from the ideal output of 1.0V or between 0.994 volts and 1.006 volts dc. This error performance is summarized in the graph of Figure 8 which shows error versus input level in the AD637K and AD536J rms-dc converters.

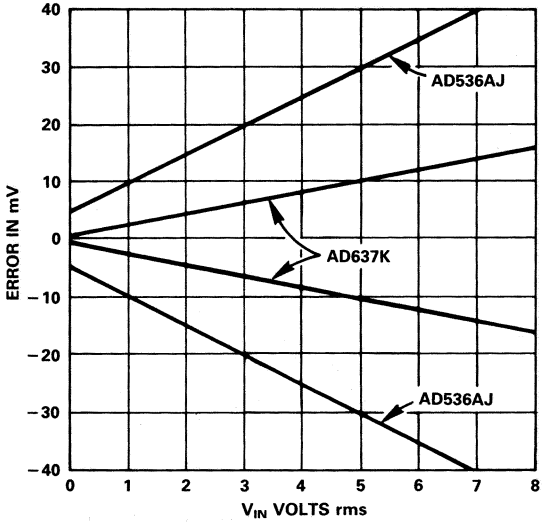


Figure 8. Maximum Error vs. Input Level AD637K and AD536AJ rms Converters.

These static errors can be classified into the standard categories of offset voltage, scale factor (gain) error, and nonlinearity errors.

Every *practical* rms converter will have an input/output transfer characteristic that deviates from the ideal. The detailed error explanation given by Figures 9a and 9b illustrates the major classes of errors which are commonly encountered. At low levels, the rms converter's input offset voltages can flatten the point of the ideal absolute value transfer and shift it up (or more positive) from the zero output voltage level with zero input voltage applied (see Appendix A). The practical effects of these offset errors determine both the resolution and accuracy of the converter for low level input signals.

For the ICs discussed in this guide, the combined total of offset errors is typically less than 1mV (refer to the data sheets for maximum specs). At higher input levels, those in the order of few hundred millivolts, scale factor and linearity errors may dominate offset errors. A scale factor error is defined as the difference between the average slope of the actual input/output transfer and the ideal 1 to 1 transfer, i.e., if a 100mV rms change in input voltage produces a 99mV change in output level, then the scale factor error is − 1%.

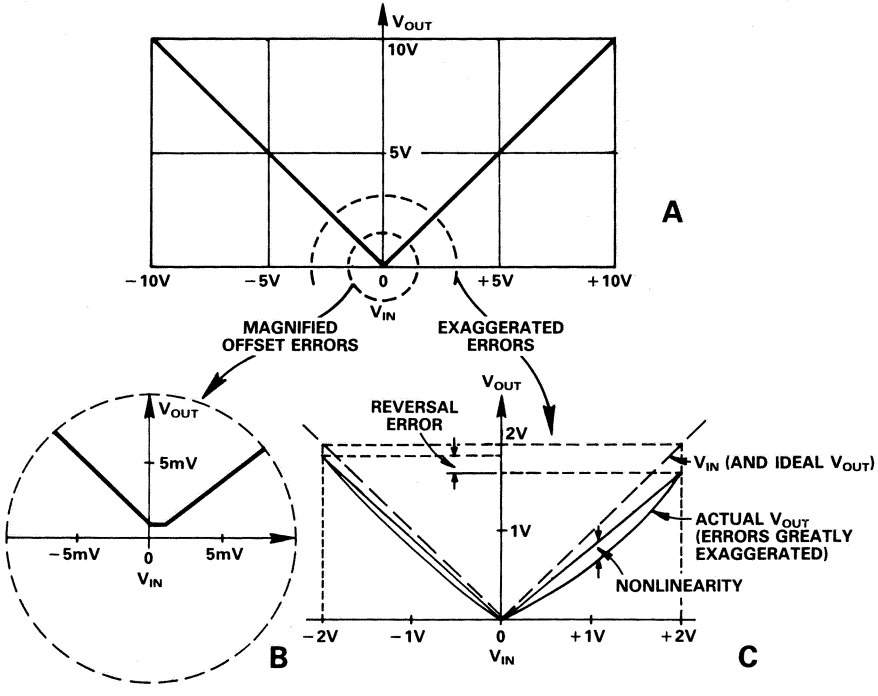


Figure 9. Static Errors in rms to dc Converters

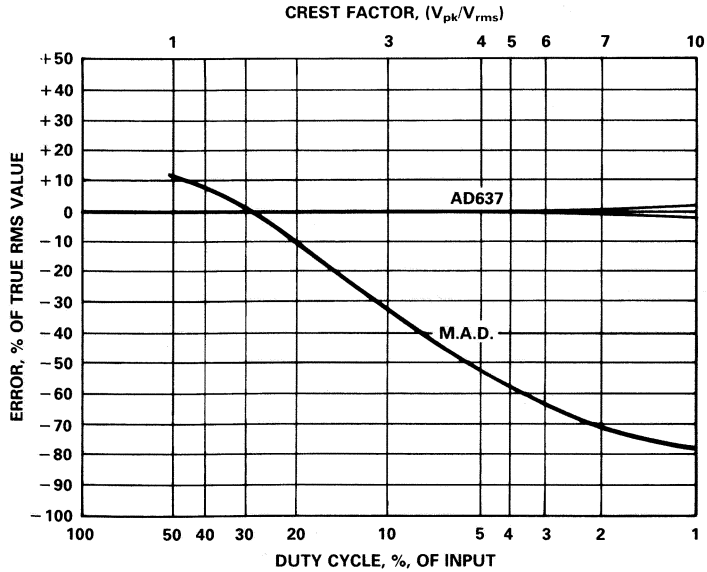


Figure 10. Error vs. Duty Cycle AD637 rms Converter and MAD ac Detector

In addition to the single polarity example just given, there can be a different scale factor for both negative and positive input voltages. The difference in these scale factors, termed the "dc reversal" error, is shown in Figure 9c. When testing this parameter, a dc voltage is applied to the converter's input, say +2V, and then the polarity of the input voltage is reversed (to −2V); the difference in the two readings will equal the dc reversal error. That is:

$$\text{dc reversal error} = \frac{(V_{OUT} + 2V\,\text{INPUT}) - (V_{OUT} - 2V\,\text{INPUT})}{2\,\text{VOLTS}} \times 100\%$$

The last remaining "static error" term is nonlinearity. As its name implies, it is the curved portion of the input/output transfer characteristic; this is shown in an exaggerated form in Figure 9c. This error is due to nonideal behavior in the rms computing section *and cannot be reduced by trimming offset or scale factor*. Therefore, nonlinearity sets a limit on the ultimate best-case accuracy of the rms converter. The nonlinearity of the AD637 is typically better than 1mV (0.05%) over a 2V full scale rms range; for the AD536A the nonlinearity equals 5mV or less. The AD636 typically has less than 1mV nonlinearity over its 0 to 200mV specified input range.

As shown by Figure 10, the errors of true rms to dc converters, although varied, are considerably lower than those errors found in precision "MAD" rectifiers when the duty cycle of the input waveform is varied.

Bandwidth Considerations

So far, we have focused on errors for response to dc inputs, yet in practice ac inputs are of the most interest to users of rms converters.

For the case of 1kHz sinewave inputs, there is negligible difference between readings at this frequency and performance with dc voltages applied, i.e., the 1kHz performance is very close to that of the static error performance with dc inputs so that dc measurements provide a convenient means of determining errors at ≈1kHz input frequencies. At higher input frequencies, however, the bandwidth characteristics of the rms converter become most important. As shown by Figures 11, 12, and 13, ac bandwidth drops off as the input level is reduced; this is primarily due to gain-bandwidth limitations in the absolute value circuits. The AD637 and AD636 both achieve greater bandwidths on low level signals than the AD536A. The AD637 maintains this advantage at levels of one volt and above; while the AD636 is limited to 200mV full scale (its low level bandwidth is greater than the AD536A and it does have overrange

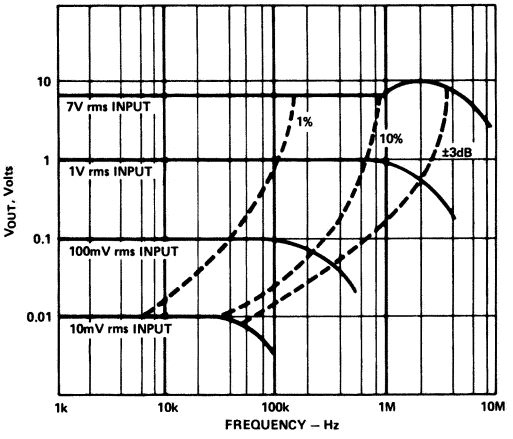


Figure 11. AD536A High Frequency Response

operation to one volt with some degradation of accuracy.)

To achieve the maximum bandwidth for a particular application, the input signal of the system or instrument being used should be amplified (or attenuated) so that the maximum rms signal level corresponds to the rms converters full scale input level. The AD536A and the AD637 can be used at up to 7 volts full scale, however, a 2 volt full scale range allows for more headroom on peak inputs (high crest factor signals). These are usually limited by the clipping level of the input preamplifier to ± 12 volts. The AD536A and AD637 will not clip with up to ± 20 volt signals. Nevertheless, a 7 volt rms input signal with a crest factor of only 3 will have a 21 volt peak input level– overloading these devices! Therefore, caution should always be used when designing rms measuring systems which must deal with complex waveform amplitudes above 1 volt rms.

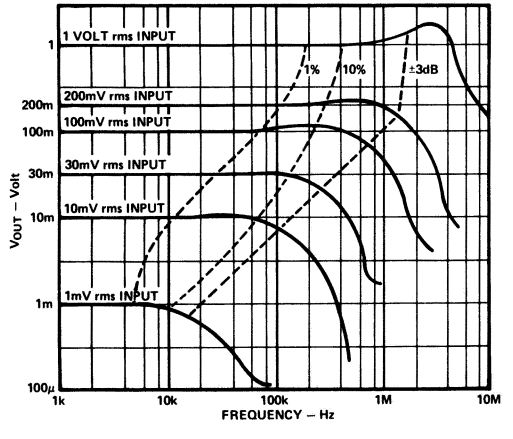


Figure 12. AD636 High Frequency Response

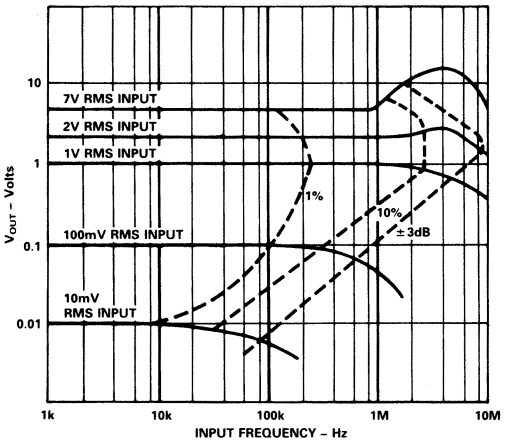


Figure 13. AD637 High Frequency Response

EXTERNAL OFFSET AND SCALE FACTOR TRIMMING

Introduction

External trimming is recommended for those applications requiring the lowest possible offset and scale factor errors. External offset trimming will improve the overall dynamic range of the device, until limited by the input offsets in the absolute value section. Regulated power supplies are recommended with any external trim scheme, since supply variations will affect the long-term accuracy of offset adjustments.

Normally, the external scale factor trim should be adjusted at the EXPECTED full scale rms voltage level for the particular application. However, it is important to point out that each of the three rms converters featured in this guide is internally laser trimmed at a specific input level. This equals 7 volts rms for the AD536A, 2 volts for the AD637, and 200mV for the AD636; this is NOT the maximum full scale level each device is capable of handling! Rather, like so many aspects of engineering, there is a design tradeoff between accuracy of an rms converter at full scale and its maximum error at lower input levels. For example, the AD536A scale factor is pretrimmed at the 7 volts rms level. If it is externally trimmed at 2 volts rms, the zero to two volts accuracy will be improved and if properly trimmed, there will be NO error at exactly 2 volts rms; however, the ab-

solute accuracy at the 7 volts rms level will now be reduced.

AD536A

Referring to Figure 14, the AD536A output offset trim is accomplished by adjusting trimmer R_4; this causes current to flow through the resistor divider formed by resistors R_3 and R_2. The resultant offset voltage developed across resistor R_2 adds to or subtracts from the output voltage at pin 8.

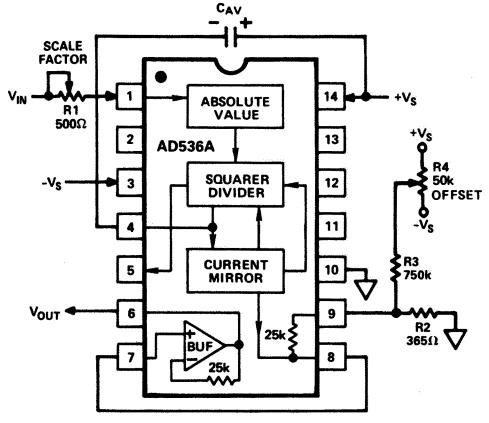


Figure 14. AD536A External Offset and Scale Factor Trimming

Scale factor trimming is performed by inserting a 500Ω trim potentiometer in series with the input terminal, pin 1. To compensate for the reduction in scale factor caused by the series trimmer, a 365Ω resistor is placed in series with the 25kΩ current mirror load resistor, appearing at pin 9. This raises the gain such that there is zero scale factor change with the trimmer set to the middle of its range. The range of scale factor adjustment is ± 1.5%.

AD636

Trimming the output offset and scale factor of the AD636 is performed in exactly the same manner as with the AD536A; however, the external component values differ, as shown by Figure 15.

AD637

Figure 16 shows external offset and scale factor connections for the AD637. Two external components are required for scale factor adjustment: scale factor trimmer R_1, inserted between the V_{OUT} pin and the denominator input pin, LOWERS the denomination

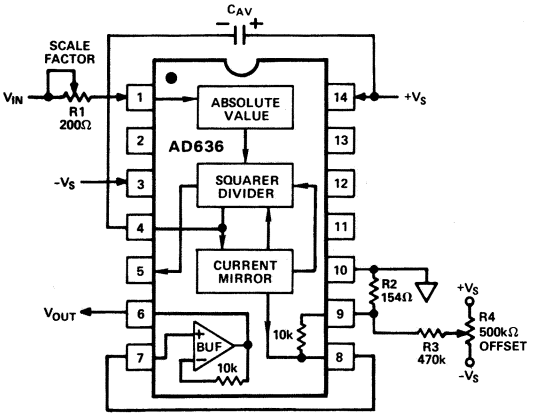


Figure 15. AD636 External Offset and Scale Factor Trimming

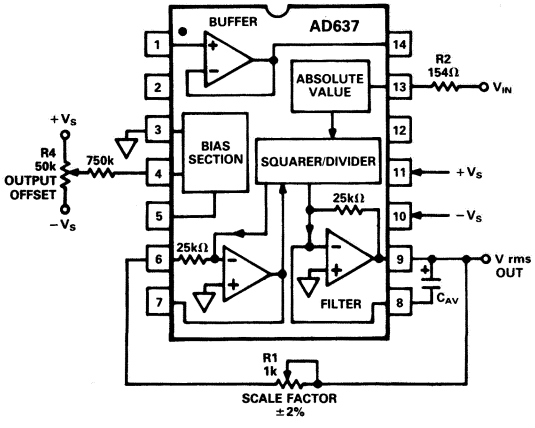


Figure 16. AD637 External Offset and Scale Factor Trimming

input voltage thus RAISING the scale factor of the device. The second required component, series resistor, R_2, lowers the rms converter's scale factor enough so that there is zero scale factor change with trimmer R_1 set (approximately) in the center of its range.

Recommended Trimming Procedure (All Three Devices)

1. Ground the signal input point, V_{IN}, and adjust trimmer R_4 for an output of zero volts. Alternately, R_4 can be adjusted to give the correct output with the lowest expected value of V_{IN} applied. This second method allows the lowest possible error over the expected input range, but results in higher errors below this range.

2. Connect the desired full scale input level to V_{IN}, using a 1kHz calibrated ac voltage source. Then adjust trimmer R_1 to give this output voltage; i.e., V_{OUT} should equal V_{IN}. This adjustment will give specified accuracy with a 1kHz sinewave input and slightly less accuracy with other input waveforms.

With correct external offset and scale factor trimming, the remaining errors in an rms converter will be due to nonlinearity effects of the device; unfortunately, nonlinearity errors cannot be reduced by external trimming (see accuracy of rms to dc converters section).

FILTERS AND AVERAGING

Introduction

RMS converters are capable of accurately measuring the rms value of both the dc and the ac components of an input signal. Unfortunately, as with all real (nontheoretical) measuring devices, accuracy needs some qualification or detailed explanation. It is, therefore, useful to understand the sources of these errors to optimize an rms converter's performance for a particular application, and as with all real systems, some design trade-offs are necessary.

Averaging and Filtering Time Constants

There are two major design decisions required:

1) Choosing the averaging time constant
2) Choosing the post filtering time constant

The averaging time constant τ_1 will equal:

$$\tau_1 \text{ in seconds} = \frac{0.025 \text{ seconds}}{\mu F} \times C_{AV}$$

for a $1\mu F$ C_{AV} τ will equal:

$$\frac{0.025 \text{ seconds}}{\mu F} \times 1.0\mu F$$

$= 0.025$ seconds or 25ms

Since the averaging time is the time in which the rms converter "holds" the input signal during computation, it directly affects the accuracy of the rms measurement.

DC Error and Output Ripple

Figure 17 shows the typical output waveform of an rms converter with a sinewave input applied. In reality, the ideal value ($V_{OUT} = V_{IN}$) is never actually achieved; instead, the output contains both a dc and an ac error component.

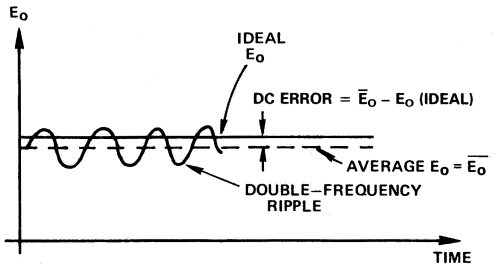


Figure 17. Typical Output Waveform for Sinusoidal Input

For an rms converter with negligible offset, scale factor, and linearity errors: the dc error component is the difference in dc volts between the average of the output signal (average E_o line of Figure 17) and the ideal output (ideal E_o). Mathematically, this equals:

$$\text{DC ERROR (in \% of reading)} = \frac{1}{0.16 + (6.4\tau_1^2F^2)}$$

where $\tau_1 = 0.025 \dfrac{\text{seconds}}{\mu F} \times C_{AV}$

F = Input frequency in Hz

The ac component of output error is present in the form of an output ripple whose frequency is double that of the input signal (for symmetrical waveforms). The peak value of the output ripple equals:

$$\text{PEAK RIPPLE } \underline{C_{AV}} \text{ ONLY (in \% of reading)} = \frac{50}{\sqrt{1 + (40\tau_1^2F^2)}}$$

As a practical example, using the circuits of Figures 18 and 19:

An input frequency of 60Hz and $1\mu F$ C_{AV} will give a dc error of . . .

$$\frac{1}{0.16 + (6.4 \times (0.025)^2 \times (60)^2)} = 0.0687\%$$

The peak output ripple for these same conditions will equal . . .

$$\frac{50}{\sqrt{1 + (40 \times (0.025)^2 \times (60)^2)}} = 5.241\%$$

The ac error or ripple may be easily removed at the output of the converter by a simple low pass filter

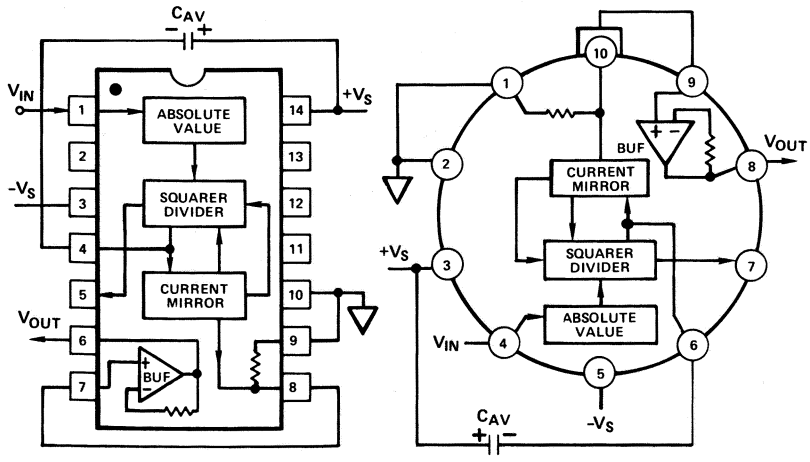


Figure 18. AD536A/AD636 Standard rms Connection

(see Figures 25 and 26). But, in contrast,the dc error is set by the averaging time constant *alone* and *cannot* be reduced by post filtering. This becomes apparent by noticing that even a perfectly averaged output that might be achieved by using a very large output filter (the average E_o line of Figure 17) still never approaches the ideal value.

Keep in mind that the dc error will be less than 0.2% of reading for sinewave inputs with frequencies greater than $1/\tau$ (for example $\geqq$40Hz for τ = 25ms) and that the error varies as $1/F^2$.

In practical terms, this means that as the input frequency doubles, the dc error reduces to 1/4 of its original value and rapidly becomes insignificant as the input frequency is raised further.

Since there are two components of averaging error, (dc error and ripple) at the converter's output, the exact nature of the devices following it become important. For example, some applications are entirely or predominantly insensitive to output ripple: analog meter movements, and meters which have hardware or software averaging carried out within them are good examples. For such cases, only the magnitude of the dc error is important.

For other devices, such as digital meters without internal averaging, the dc and ac components both add to the uncertainty of the measurement with the maximum uncertainty or "averaging error", equal to the *peak* value of the output ripple plus the dc error.

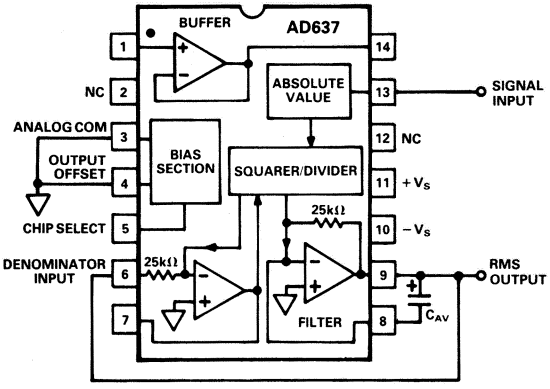


Figure 19. AD637 Standard rms Connection

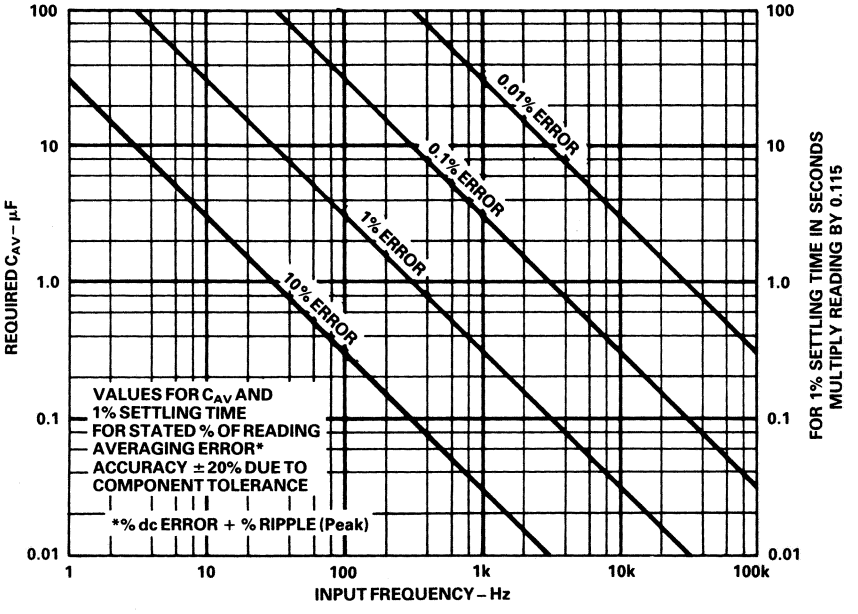


Figure 20. Error/Settling Time Graph for Use with the Standard rms Connection

The Standard RMS Connection

Figure 20 gives practical values of C_{AV} for various values of averaging error over frequency for the standard rms connections (no post filtering) of Figures 18 and 19. The standard rms connection has the advantage of requiring only one external component.

Design Considerations – Error Versus Ripple

As previously stated, if the devices following the converter are ripple sensitive, the ripple must be reduced, optimally *at least* below the level of the dc error.

A comparison of the left-hand bar to that of the dotted line of Figure 21 shows that the error due to the output ripple using a C_{AV} only is considerably larger than that due to the dc error. For example, the peak ripple at 50Hz is sixty-three times the level of the dc error when no post filter is used, i.e., 6.3% ripple versus 0.1% dc error (both specified in % of reading).

This graph dramatically shows the effectiveness of a post filter in reducing overall averaging error. Note: when using C_{AV} alone, the output ripple constitutes over 99% of the total averaging error; for the one pole filter case using C_2 equal to 3.3 times C_{AV}, the ratio is close to 50/50, and for a 2 pole filter with C_2 and C_3 equal to 2.2 times C_{AV}, the dc error is the main source of error, contributing to approximately 95% of the averaging error.

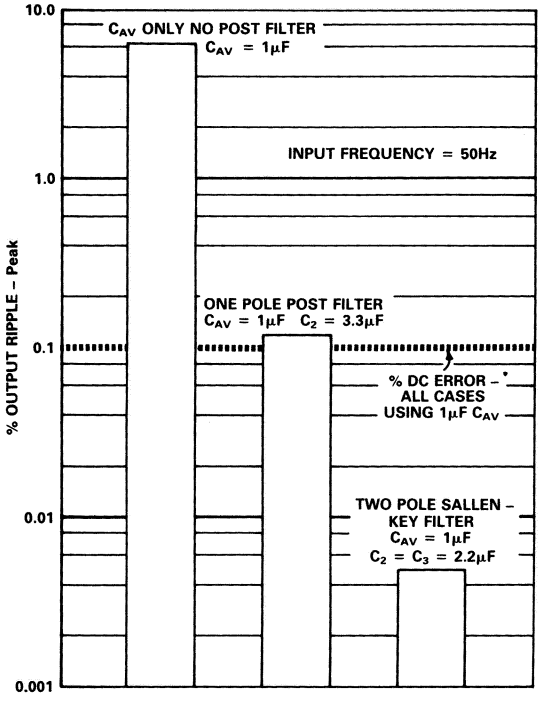


Figure 21. Comparison of the Level of dc Error to that of the Ripple Amplitude – AD536A/AD637 (for AD636 Multiply Values of C2 & C3 by 2.5)

The addition of a single capacitor to the output of the rms converter (see Figures 25 and 26), in this case with a value of 3.3μF, will reduce the output ripple to 0.12%–almost fifty-three times. A two pole filter, shown by the right hand bar of Figure 21, reduces the ripple (and overall averaging error) still further. Of course, the 50Hz ripple could be reduced to the 0.1% level by increasing C_{AV} fifty-three times– to 53μF. Unfortunately, this not only gives values of C_{AV} that may be physically too large, but it creates another problem–excessively long averaging and settling time constants (see the following section for an explanation of settling time).

Filtering Versus Settling Time

Settling time (t_S) is defined as the time required for an rms converter to settle to within a given percent of the change in rms level. The relationship between the value of C_{AV} and output settling time is set by the averaging time constant and varies 2 to 1 between increasing and decreasing input signals. Increasing input signals require 2.3 time constants to settle or:

$$ts = 2.3 \times (0.025 \frac{\text{seconds}}{\mu F} \times C_{AV})$$

to within 1% of the *change* in rms level. Decreasing signals require 4.6 time constants:

$$ts = 4.6 \times (0.025 \frac{\text{seconds}}{\mu F} \times C_{AV})$$

to within 1% of the *change* in rms level.

This translates into 57.5ms per μF C_{AV} for increasing signals and 115ms per μF for decreasing signals. For most applications, the 115ms per μF figure should be used, therefore providing the worst case settling time.

Note: The formulas, graphs, and computer programs in this application guide all establish the worst case (or decreasing amplitude) settling times.

Settling Time versus Input Level–AD536A and AD636 Only

In addition to the 2:1 difference in settling time for increasing and decreasing signals, the AD536A/AD636 settling time will also vary with input signal level, increasing as the input level is reduced, as shown in Figures 22 and 23.

Note: The AD637 settling time is constant with input signal level, dependent only on the value of C_{AV}.

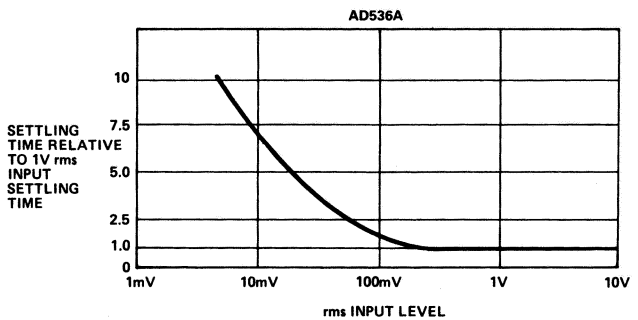


Figure 22. AD536A Settling Time vs. Input Level

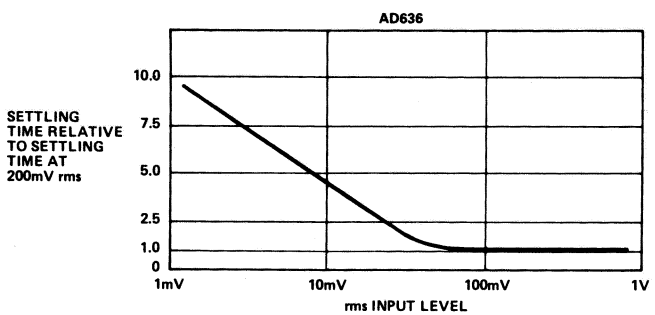


Figure 23. AD636 Settling Time vs. Input Level

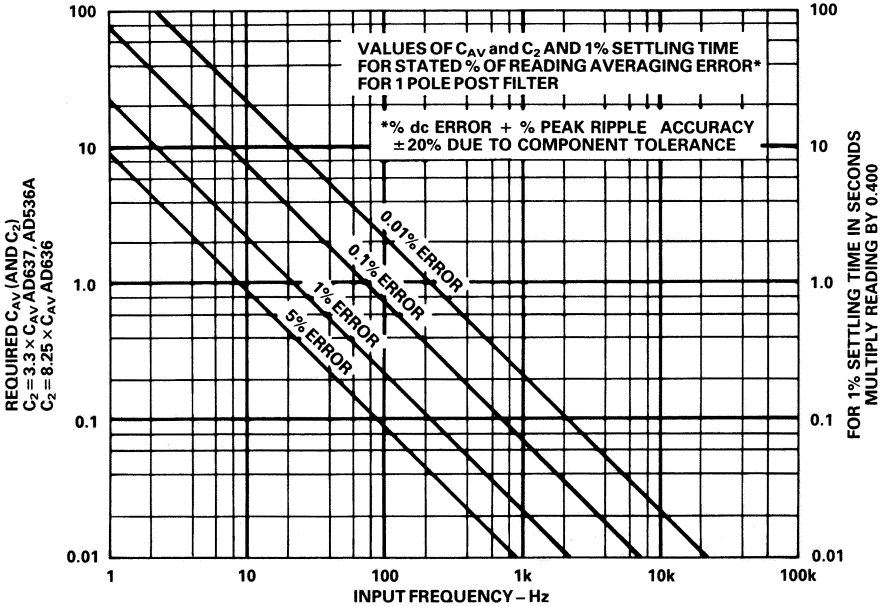


Figure 24. Error/Settling Time Graph for Use with 1 Pole Output Filter Connection

Using A One Pole Output Filter to Reduce Ripple and Overall Settling Time

For the 53μF C_{AV} example, the time required for the output to settle to within 1% (of the change in rms level) would equal *5.3 seconds*! For most applications, it's far better to pick a value of C_{AV} just large enough to give the desired maximum dc error at the lowest frequency of interest and use post filtering to remove the excess ripple. For the one pole post filter, the best overall compromise between averaging error and settling time occurs with the value of C_2 equal to 3.3 times the value of C_{AV}. Figure 24 gives recommended capacitance values using these ratios. Settling time *does* increase with the addition of this extra capacitor, but the increase is much less than if ripple had been reduced using C_{AV} alone. For a one pole output filter, the total worst case settling time will equal the root sum squares of the averaging and filtering time constants.

$$ts = \sqrt{(4.6\tau_1)^2 + (4.6\tau_2)^2}$$

where

$$\tau_1 = 0.025 \frac{\text{second}}{\mu F} \times C_{AV}$$

$$\tau_2 = 0.025 \frac{\text{second}}{\mu F} \times C_2$$

For example: Using the circuits of Figures 25 and 26, a 1μF C_{AV} and a 3.3μF C_2 will give a total settling time of . . .

$$ts = \sqrt{(0.115)^2 + (0.3795)^2} = 0.39655 \text{ seconds}$$

or 396.5ms

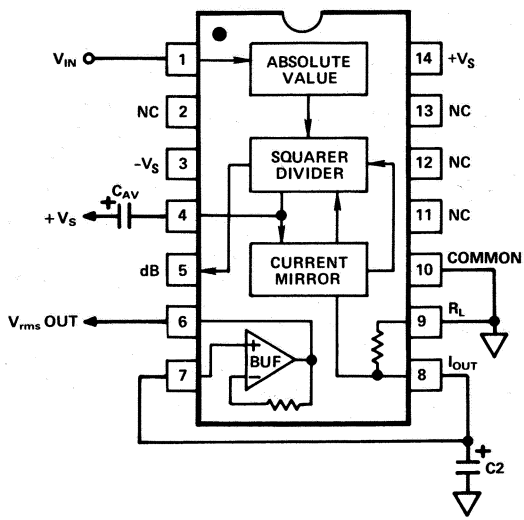


Figure 25. AD536A/AD636 with a 1 Pole Output Filter

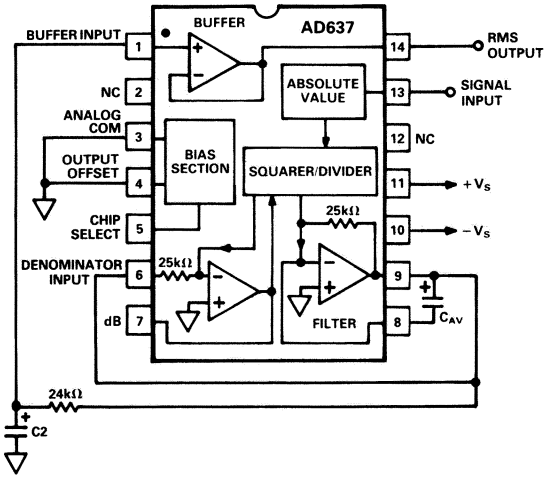


Figure 26. AD637 with a 1 Pole Output Filter

The total 1% settling time for this example is only one thirteenth of that required for a 53μF C_{AV} using the standard rms connection, yet the one pole filter provides the same reduction in output ripple.

The formula for computing output ripple using the one pole filter circuits of Figures 25 and 26 is:

$$\%\ \text{ripple} = \frac{50}{\sqrt{1 + 40\tau_1^2F^2}} \times \frac{1}{\sqrt{1 + (4\pi F)^2(\tau_2)^2}}$$

where $\tau_1 = 0.025\frac{\text{sec}}{\mu\text{F}} \times C_{AV}$

$\tau_2 = 0.025\frac{\text{sec}}{\mu\text{F}} \times C_2$

F = Input signal frequency

Note: For automatic computation of error, ripple, and settling time using the Apple II computer, see Appendix C.

Settling Time Approximations When Using a Post Filter

Referring to the one pole filter example: notice that when the rms converter is followed by a post filter, in this case with a recommended time constant 3.3 times that of the averaging section, the post filter dominates the overall settling time of the circuit. This effect also takes place when using a two pole output filter in which each section has a time constant 2.2 times (or more) than that of the averaging section. Therefore, when using a post filter, the total settling time may be approximated to within 5% error by determining the post filter settling time alone.

For a one pole filter case using a 1μF C_{AV} and a 3.3μF C_2, ts of the output filter will equal: 0.025 seconds/μF times 3.3μF times 4.6 time constants = 397.5ms. Note how close 397.5ms is to the *exact* figure of 396.5ms which was previously calculated by finding the square root of the sum of squares!

Table 3 shows the basic formulas which determine the required settling time constants for the rms section to settle to within various percentages of the new rms level when undergoing a step change in input level. The values in brackets are those of a linear RC filter. As shown by the table, there is a consistent two to one difference in settling time between increasing and decreasing signals in the averaging section of the rms converter.

	For Increasing Amplitudes	For Decreasing Amplitudes
Basic Formulas	$\Delta V\sqrt{1-e^{-T/RC}}$	$\Delta V\sqrt{e^{-T/RC}}$
Settling Time to Within Stated % of New rms Level		
1%	2.0τ (4.6τ)	4.6τ (4.6τ)
0.1%	3.1τ (6.9τ)	6.9τ (6.9τ)
0.01%	4.2τ (92τ)	9.2τ (9.2τ)
( ) indicates settling time for linear RC filter		

Table 3. Number of RC Time Constants (τ) Required for AD536A, AD636, AD637 rms Converters to Settle to Within Stated % of Final Value

The Two Pole Output Filter

Referring again to Figure 21, a further reduction in output ripple and, therefore, overall averaging error may be achieved by using a two pole Sallen-Key filter shown in Figures 27 and 28. The resistor and capacitor ratios in these filters were chosen to provide a Butterworth or flat amplitude versus frequency response.

Figure 21 shows that with the two pole output filter, the predominant component of averaging error is the dc error. In fact, in this case, the dc error is twenty times greater. The % ripple output of the two-pole Sallen-Key filter will equal the ripple input to the filter (from the rms converter output) times the transfer function of the Sallen-Key filter.

$$\% \text{ ripple} = \frac{50}{\sqrt{1 + 40\,\tau^2F^2}} \times \frac{\left(\frac{1}{\tau_2}\right)^2}{\sqrt{\left[\left(\frac{1}{\tau_2}\right)^2 - (4\pi F)^2\right]^2 + \left(\frac{8\pi F}{\tau_2}\right)^2}}$$

where: $\tau_1 = 0.025 \frac{\text{seconds}}{\mu F} \times C_{AV}$

$\tau_2 = 0.025 \frac{\text{seconds}}{\mu F} \times C_2$

$C_2 = C_3$

F = Input signal frequency in Hz

For automatic computation of dc error, ripple, averaging error, and settling time using the Apple II computer, See Appendix C. As with the other rms connections, averaging error may be determined via the computer program, by using the formulas directly, or in this case, by referring to Figure 29.

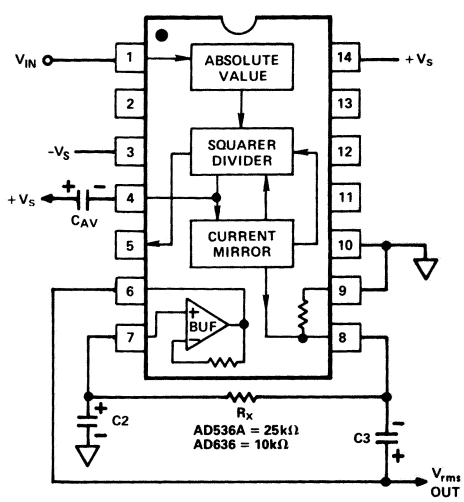


Figure 27. AD536A/AD636 with a 2 Pole Output Filter

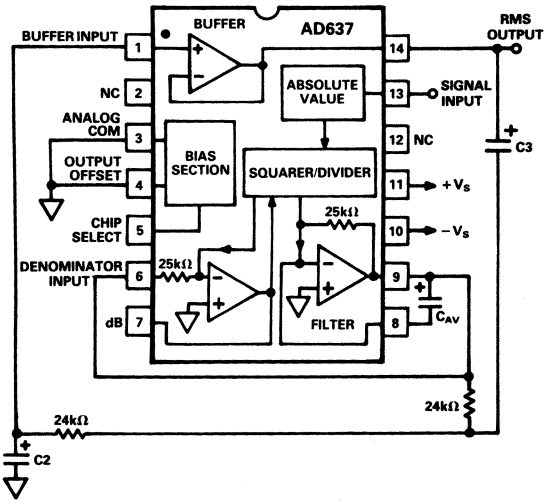


Figure 28. AD637 with a 2 Pole Output Filter

The *exact* 1% settling time (worst case) for the two pole post filter circuit equals the root sum squares of the settling time due to C_{AV} plus the settling times of each pole of the filter. That is:

$$\text{ts two pole output filter} = \sqrt{(4.6\tau_1)^2 + (4.6\tau_2)^2 + (4.6\tau_3)^2}$$

where: $\tau_1 = 0.025 \frac{\text{seconds}}{\mu F} \times C_{AV}$

where: $\tau_2 = 0.025 \frac{\text{seconds}}{\mu F} \times C_2$

where: $\tau_3 = 0.024 \frac{\text{seconds}}{\mu F} \times C_3$

Note: As with the one pole filter, the circuit settling time may be very closely approximated (to within 5%) by calculating the settling time of the post filter alone. For a two pole filter, this equals 1.4 times the time constant of either section times 4.6 time constants (for $C_2 = C_3$). Using a 1μF C_{AV}–2.2μF C_2, C_3 example, the approximate circuit settling time to 1% will equal: ts = 1.4 × 0.025 second/μF × 2.2μF × 4.6 = 354.2ms.

DETERMINING THE COMBINED ERROR OF THE RMS MEASURING SYSTEM

The total worst case error of an rms circuit will be the sum of all its individual errors. To closely approxi-

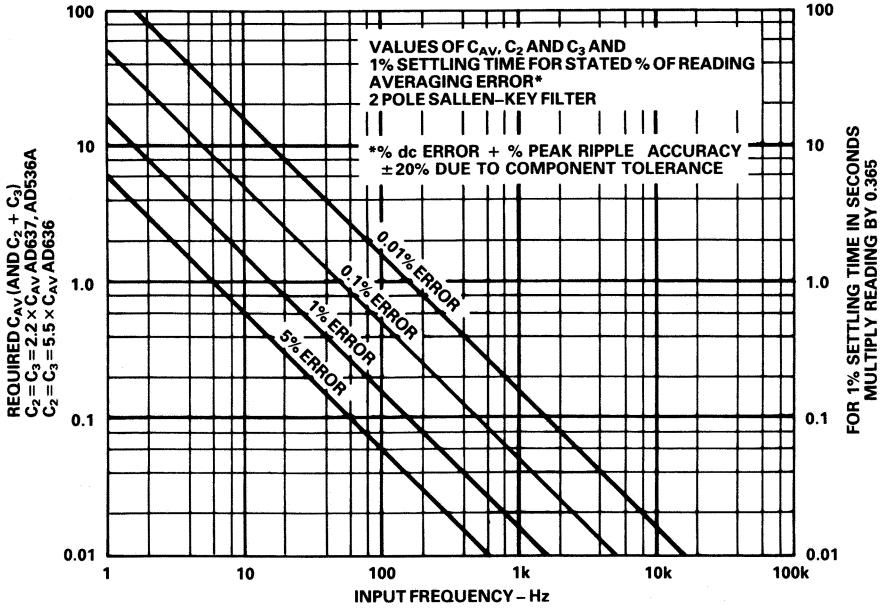


Figure 29. Error/Settling Time Graph for Use with 2 Pole Output Filter

mate this *combined* error, first decide on whether or not an output filter is needed: then select an appropriate value of C_{AV} (and C_2 and C_3 if they are used). Go to the appropriate graph and find the averaging error at the lowest frequency of interest. Add this to the "total error internal (or external for an externally trimmed circuit) trim" spec. The combined error is then the maximum *worst case* error the system will produce, even though in most cases performance will be better. (In particular, performance will always improve as the input frequency increases.)

Note: If all of this sounds confusing, try this cookbook approach:

Select the "J" grade part, take its "total error" spec, and add 1% to it. If this gives too great a combined error, go to the "K" grade part or provide for external trimming and use that improved spec. Go to the one pole post filter graph and find the lowest frequency of interest. Then find the value of C_{AV} from where the 1% averaging error line intersects with the frequency line. (If settling time is *not* a problem, use the 0.1% averaging error lines on the charts.)

Once the value of C_{AV} is known, C_2 is found by multiplying the value of C_{AV} by: 3.3 for the AD637 and AD536A, or 8.25 for the AD636. Total settling time for the system is the point on the right hand vertical axis directly across from the C_{AV}, C_2 scale. If settling time is found to be too great, it may be reduced (approximately 30%) by using a two pole post filter. For this case, use the two pole filter graph, find the new values for C_{AV}, C_2, and C_3 and the corresponding settling time for the circuit.

For specific details concerning very low frequency rms measurement refer to pages 37–39.

USING THE INTERNAL BUFFER AMPLIFIER TO ISOLATE THE FILTERING CIRCUIT

The primary use of the AD536A/AD636 internal buffer amplifier is as an output buffer in its standard output configuration. The obvious advantage of using an output buffer is to isolate the filtering circuit (capacitor C_2 and internal load resistor R_L), from external loads being driven by the rms converter (see Figure 27). Unless these loads are *very* high impedance, they will adversely affect both the scale factor accuracy and the filtering performance of the rms converter. The $10^8\Omega$ buffer input impedance allows the output filter to operate independent of any external loading effects.

Note: Since the AD637 has a low impedance output, its internal buffer amplifier may not be required. For design considerations concerning the use of either the AD536A or AD636 with its internal buffer amplifier serving as an input buffer, see Appendix B.

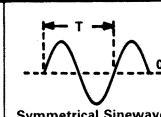
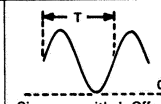
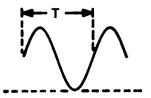
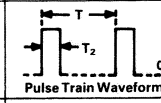
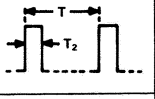
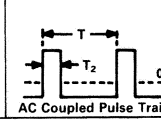
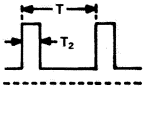
THE EFFECTS OF THE SYMMETRY, DC OFFSET, AND DUTY CYCLE OF INPUT WAVEFORMS ON THE REQUIRED VALUE OF C_{AV}

The selection of averaging capacitor value given in the previous sections was based on the input signals being symmetrical (sine, triangle, or square) waveforms. If asymmetrical waveforms or low duty cycle pulse trains are applied to the input of an rms, converter, the total averaging time (and, therefore, the value of C_{AV}) required will increase.

The reason for this increase becomes apparent by referring to Figure 35. As shown by the figure, the averaging takes place at the C_{AV} terminal, a point in the circuit *after* the absolute value circuit. The absolute value circuit full wave rectifies the input signal–effectively doubling the input frequency (if the input waveform is symmetrical). It is, therefore, important to consider the input waveform as it appears after full wave rectification when deciding on the value of C_{AV}. Table 4 illustrates this point and gives averaging time constant ratios for various types of input waveforms. In addition, practical component values for 60Hz input signals are also specified.

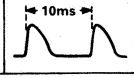
Note: For frequencies other than 60Hz, capacitance values may simply be ratioed (i.e., 30Hz = 2 × 60Hz values, 120Hz = 1/2 60Hz values) or calculated using the new R × C_{AV} averaging time constants.

Table 5 gives practical component values for SCR type input waveforms with frequencies of 50Hz and 60Hz.

	Input Waveform and Period	Absolute Value Circuit Waveform and Period	Minimum R × C_{AV} Time Constant	Recommended C_{AV} and C2 Values for 1% Averaging Error@60Hz with T = 16.6ms			1% Settling Time
				C_{AV} as Calculated	Recommended Standard Value C_{AV}	Recommended Standard Value C2	
A	 Symmetrical Sinewave		1/2T	0.33μF	0.47μF	1.5μF	181ms
B	 Sinewave with dc Offset		T	0.66μF	0.82μF	2.7μF	325ms
C	 Pulse Train Waveform		10(T − T_2)	5.98μF for T_2 = 0.1T	6.8μF	22μF	2.67sec
D	 AC Coupled Pulse Train		10(T − 2T_2)	5.31μF for T_2 = 0.1T	5.6μF	18μF	2.17sec

VALUES ARE SPECIFIED FOR AD536A AND AD637. FOR AD636 MULTIPLY C2 VALUES BY 2.5.

Table 4. A "Cookbook" Capacitor Selection Chart for Various Input Waveforms

Input Frequency and Period	Absolute Value Circuit Waveform and Period	C_{AV} Value			C_2 Value (3.3 × C_{AV})			1% Settling Time
		Calculated Value for 10 Time Constants	+20% to Provide for Component Tolerance	Closest Standard Value	Calculated Value for 10 Time Constants	+20% to Provide for Component Tolerance	Closest Standard Value	
60Hz 16.67ms		3.2μF	3.84μF	4.7μF	10.56μF	12.67μF	15.0μF	1.81sec
50Hz 20ms		4.0μF	4.8μF	5.6μF	13.2μF	15.8μF	15.0μF	1.84sec

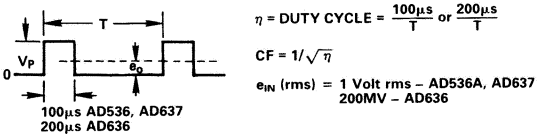
VALUES GIVEN FOR 1 POLE POST FILTER CONNECTION AD536A, AD637 FOR AD636 MULTIPLY C_2 VALUE BY 2.5

Table 5. Capacitor Selection Chart for SCR Input Waveforms for a Maximum of 1% Worst-Case Averaging Error

ERROR VERSUS CREST FACTOR

AD536A

Figure 30 provides a percent of reading error for the AD536A for a 1 volt rms input signal with crest factors from 1 to 10 (1 volt peak amplitude). A rectangular pulse train (pulse width 100μs) was used for this



test since it is the worst-case waveform for rms measurement (all the energy is contained in the peaks). The duty cycle and peak amplitude were varied to produce the various crest factors while maintaining a constant 1 volt rms input amplitude.

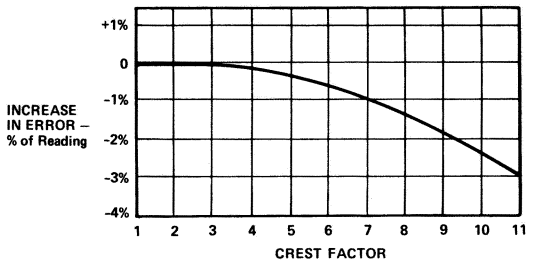


Figure 30. AD536A Error vs. Crest Factor

AD636

Figure 31 shows the error versus crest factor for the AD636 rms converter with a 200mV rms input signal applied. Crest factor range for the AD636 is from 1 to 7 (1.4 volts peak amplitude). The pulse width in this case was 200μs.

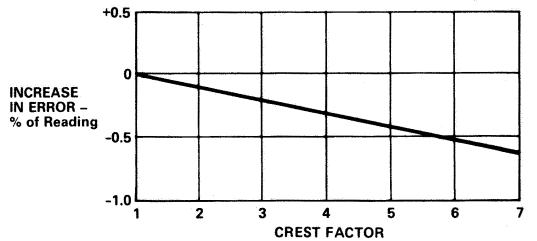


Figure 31. AD636 Error vs. Crest Factor

AD637

As displayed by Figure 32, the error versus crest factor of the AD637 will vary within the shaded portion of the graph. This variation is due to component tolerances in each chip's internal compensation network. Fortunately, the overall variation is quite small.

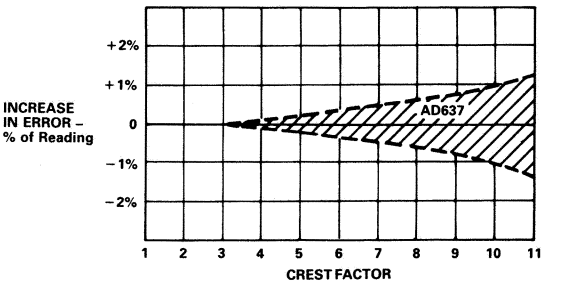


Figure 32. AD637 Error vs. Crest Factor

SINGLE SUPPLY OPERATION

AD536A

Rather than using symmetrical power supplies to operate the AD536A, a single polarity supply as low as +5 volts may be used instead. This requires biasing the AD536A common terminal (pin 10) above ground as shown in Figure 33. The ratio of two resistors, R_1 and R_2 form a voltage divider between $+V_S$ and ground. Choosing the correct bias voltage for the common terminal is a trade-off between the maximum positive vs. the maximum negative input voltage the AD536A can tolerate without clipping. For example, as resistor R_2 is made larger, pin 10 is effectively raised more above ground. This will increase the maximum negative input voltage of the AD536A while at the same time decreasing the maximum positive input voltage the rms converter

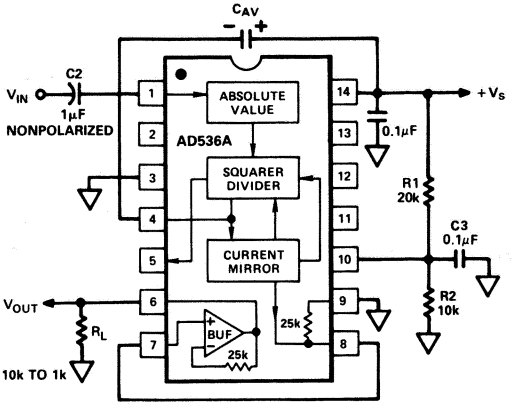


Figure 33. AD536A Single Supply Connection

can handle. The values of resistors R_1 and R_2 in Figure 33 were selected to give the best overall operation using a +15 volt supply, however, pin 10 should be at least +2 volts above ground for correct operation. The AD536A common pin requires less than 5μA of input current, therefore, the values of resistors R_1 and R_2 can be chosen so that:

$$\frac{V_{SUPPLY}}{R_1 + R_2} = 50\mu A$$

or 10× the common pin current. This permits adequate voltage stability on the common pin while still minimizing overall power consumption.

AD636

The AD636 low power rms converter may also be operated from a single power supply, in this case between +5.0V dc and +24.0V dc. The same design trade-offs apply to the AD636 as to the AD536A when choosing the optimum values for resistors R_1 and R_2, although since the AD636 was optimized to operate from unequal supplies (+3.0, −5.0V dc), the ratio of the two resistors will be different for the two devices. The values for resistors R_1 and R_2 in Figure 34 were chosen for the best overall performance using a 9 volt battery (for examples of battery operation, see dB meters section).

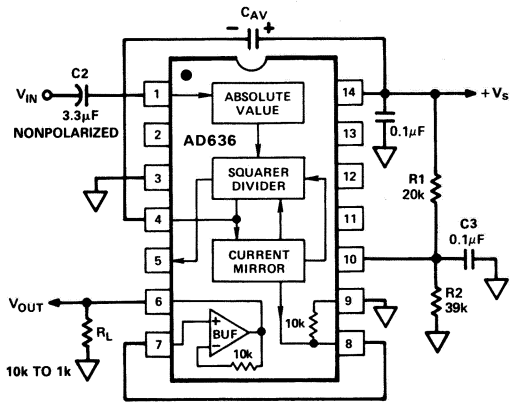


Figure 34. AD636 Single Supply Connection

AD637

The AD637 has its output voltage derived via an inverting low pass filter which does provide output buffering; however, the operational amplifiers in this filter stage will not operate down to the negative supply (as will the current mirror in the AD536A/AD636). The AD637 *can* be operated from a single supply voltage but only if its output voltage does not have to be less than 2 volts above the negative supply. Therefore, you may bias the AD637 above ground using equal value resistors (R1 & R2 with typical values of approximately 15kΩ); this allows single supply operation from power supplies between +5 volts and +36 volts dc using the same scheme shown in Figures 33 and 34. Please note: Because the filter amplifier's common pin cannot be separated from the rms converter common, the AD637 output MUST be referenced to its common pin (pin 3), NOT TO GROUND.

THE DECIBEL OUTPUT PROVISION

Basic Operating Principles

As shown by Figure 35, the dB output function originates in the squarer/divider section of the AD536A/AD636. Figure 36 shows a portion of this section redrawn to illustrate dB operation. Although component values vary, this basic scheme is common to the AD536A, AD636, and the AD637 rms converters.

The feedback current, I_3, proportional to the rms value of the input signal, is applied to the input of A_3. Transistor Q_3, in conjunction with amplifier A_3, forms a logarithmic amplifier whose output *voltage* is proportional to the natural logarithm of *current* I_3. The output of A_3, which is the V_{BE} of Q_3, is equal to:

$$V_{BE_{Q3}} = \frac{-kT}{q} \text{ Ln } \frac{I_3}{I_{ES}}$$

where $\frac{kT}{q}$ is the thermal voltage of Q_3's base emitter junction and I_{ES} is Q_3's emitter saturation current.

This output has two thermal or temperature related drift causing elements. One is a scale factor drift caused by the kT/q term which is approximately equal to 0.33% drift per degree centrigrade *at* 25°C (3300ppm/°C). The second drift term is an offset drift due to the I_{ES} of transistor Q_3. This offset varies with temperature approximately 2mV/°C.

The decibel is based on the log of the ratio of two signals, or

$$dB = 20 \text{ LOG } \frac{IA}{IB}$$

Since two currents are needed, a second current I_{REF} is introduced via a second transistor Q_5.

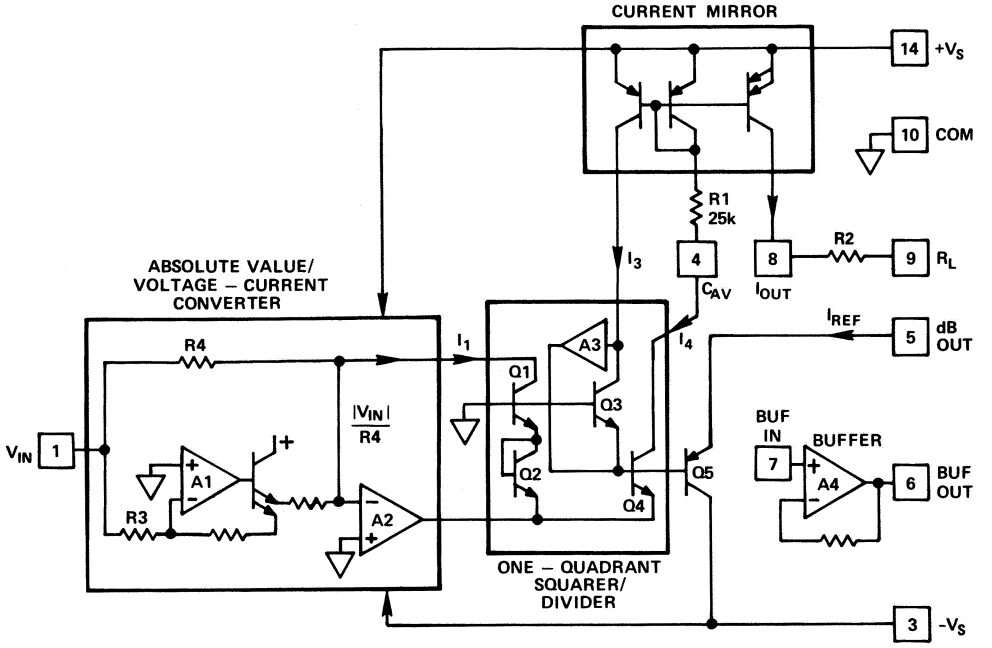


Figure 35. AD536A/AD636 Simplified Schematic

Q_5 performs several functions necessary to dB operation:

1. It performs the required division function by subtracting the logs of the two currents I_3 and I_{REF}.
2. By having its V_{BE} subtracted from the V_{BE} of Q_3, Q_3's junction offset and offset voltage drift over temperature characteristics are corrected.
3. Q_5 provides the necessary current buffering for the dB output pin.

The output voltage at the dB output terminal (via Q_5) equals:

$$\text{dB output} = (V_{BEQ3}) - (V_{BEQ5})$$

$$= \frac{-kT}{q} \text{Ln} \frac{I_3}{I_{REF}} U$$

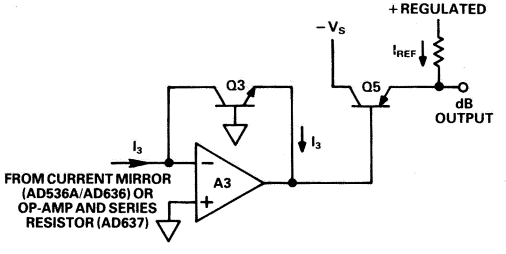


Figure 36. A Simplified Schematic of the dB Output Circuitry Common to the AD536A, AD636 and AD637 rms Converters

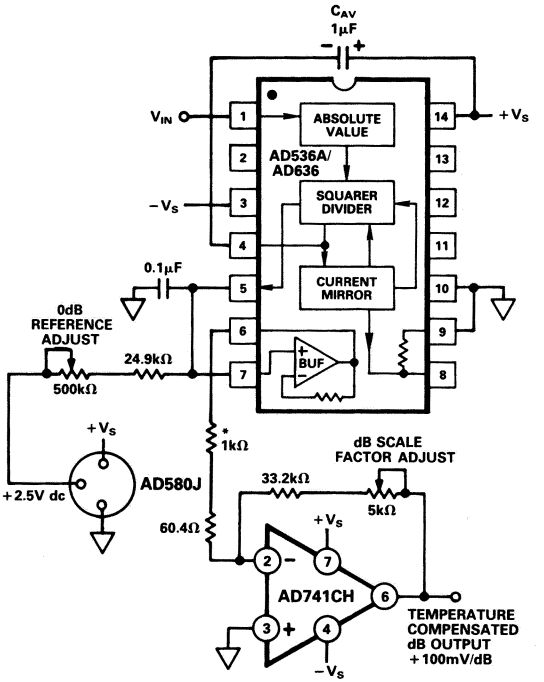
Note: U accounts for the ratio of the emitter saturation currents of Q_5 and Q_3 and also for the imperfect tracking of the V_{BE} of Q_5, a PNP transistor, with the V_{BE} of Q_3, an NPN transistor. Fortunately, for most practical applications this tracking error is negligible, as long as I_{REF} is used as a reference level *AND NOT* as a signal input.

The dB output produces an output voltage approximately equal to 3mV/dB change in I_3; it needs to be scaled and temperature compensated to be useful for most applications, (temperature compensation is required because although the offset portion of Q_3's drift has been subtracted out the 3300ppm/°C temperature drift due to $\frac{kT}{q}$ still remains). Succeeding sections will cover these requirements in detail.

AD536A/AD636 Temperature Compensation

With a temperature coefficient of 0.03dB/°C, the total error for the dB output would be ±0.3dB for a ±10°C variation in operating temperature. In many cases, this accuracy is satisfactory. However, for more critical applications, the addition of an external temperature compensating resistor is necessary.

The circuit of Figure 37 provides temperature compensation by using the averaged TC of two resistors



*SPECIAL TC COMPENSATION RESISTOR +3500ppm 1% TEL LABS Q-81 PRECISION RESISTOR CO #PT146 OR EQUIVALENT

Figure 37. AD536A/AD636 Temperature Compensated dB Output Circuit

in series to develop the desired 3300ppm. These resistors, placed between the dB output pin and the summing junction of the AD741 scale factor amplifier, change the scale factor of the circuit when temperature variations occur.

The 1kΩ +3500ppm/°C (±300ppm) TC resistor in series with a 60.4Ω 1% metal film resistor together form a 1.06kΩ +3300ppm resistor, the exact TC needed. The metal film resistor is ±50ppm and may be considered "zero" TC compared with the +3500ppm/°C resistor. The metal film resistor therefore degrades or reduces the TC resistors +3500ppm/°C by the ratio of their resistances, in this case by 6.04%.

$$\frac{60.4\Omega}{1000\Omega} \times 100\% = 6.04\% \quad 3500\text{ppm} \times 0.94$$

$$(94\%) = 3290\text{ppm/°C}$$

AD637 Temperature Compensation

This scheme, shown by Figure 38, is basically the same circuit as Figure 37. In both circuits, the output amplifier gain is set to give a 100mV output per dB change in input level.

This circuit outperforms that of Figure 37, providing a −3dB bandwidth of 4MHz with a 1V rms input level. It operates over a 70dB range from +10dB to −60dB ±2.5dB with a 0dB reference level of 1 volt rms. The 0dB reference point may be varied ±10dB from the nominal 1 volt level by using the 500kΩ 0dB adjust trimpot; however, if higher resolution is required (using 0dB = 1 volt rms) a 100kΩ trimpot may be substituted.

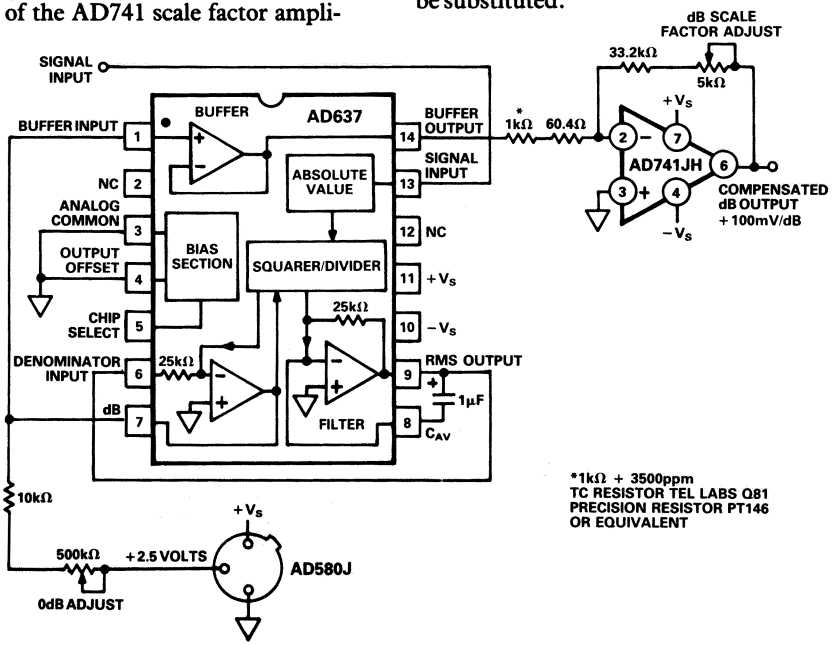


Figure 38. AD637 Temperature Compensated dB Circuit